Design of a Two Octave Gysel Power-Divider Using DGS and DMS

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***Abstract*— This paper proposes a two way L and S band Gysel power divider/combiner that uses line to ground resistors. Step by step methods to obtain a wide isolation and transmission bandwidth are presented. A design that uses five resistors is selected and optimized based on Quasi Newton method. Then the Defected Microstrip Structure (DMS) and Defected Ground Structure (DGS) is used to obtain better transmission and isolation in wider bandwidth. By resizing the structure to meet impedance matching, the two-way L and S band power divider is achieved. Also the optimization of the design is checked using circuit configuration. Finally, the theoretical results are validated by comparison with simulations of structure and experimental results. The simulations are found to be in good agreement with measurement results in the range of 0.7 to 4.3 GHz.**

Index Terms— optimization, design methodology, microstrip circuit, power dividers.

I. INTRODUCTION

Gysel was the first one who used Line to Ground Resistors (LGRs) in power dividers to obtain some advantages over the past designs. The well-known advantages of the Gysel power divider are, a) it can sustain higher power over the same size Wilkinson power divider, b) it has easy realizable geometry and c) better monitoring capability for imbalances at the output ports [1], [2]. These advantages are achieved by using the LGRs instead of line to line resistors. Furthermore, the important advantage of LGRs used in power dividers is on improvement of stability, when the power divider is used as part of an active circuit; if an unwanted signal or noise is produced on any port of power divider, the LGRs can dissipate it and not allow it to increase.

The problem with a Gysel power divider is the low isolation and transmission bandwidth. In [3] an optimization method is introduced to obtain a wideband power divider using the Gysel design. But limited bandwidth is still its inconveniences. The bandwidth as defined in (4) is improved in [4] and [5] up to 47.9%. Although, the multisection Wilkinson power divider has wider bandwidth [6], the advantages of Gysel power divider, by using the LGRs instead of line to line resistors, encourage the designer to design wideband Gysel power divider. In addition to the given advantages of using the

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LGRs, the Gysel power divider has less sensitivity on the places of resistors on fabrication of the circuit, and usually it has better phase matching. Ever since, a little variation between simulated and fabricated designs' resistors places can cause high phase difference on multisection Wilkinson power divider.

In [7] a new power divider is introduced that has wider transmission bandwidth using added LGRs. LGRs' arrangement is designed to convert isolation power coupling to dissipation, whilst it doesn't decrease transmission power. It will be achieved only when the impedance between the input and output of the power divider is less than between input/output and resistors. Also the impedance between the two outputs of the power divider is more than the impedance between outputs and resistors.

To obtain power divider with a better isolation in a wider bandwidth Defected Ground Structure (DGS) and Defected Microstrip Structure (DMS) can be useful. DGS and DMS are widely used to design optimized microstrip circuits and systems [8] - [14]. In [15], DGS has been used to reduce insertion loss on resistors of Wilkinson power divider. The key role of DMS and DGS is to avoid transmission between output ports and guide it between the input and outputs.

In this design, Arlon CuClad 250GT substrate with $\epsilon_r = 2.55$ is used and the dimensions and the values of resistors are determined through optimization based on Quasi Newton method. The optimization is implemented on the three stages of the simulation of the design, initial structure, adding DMS and adding DGS. To ensure that the design is entirely optimized a circuit configuration and optimization is also presented. The result is the 60% bandwidth for the isolation and transmission that is not achieved before as the knowledge of the authors.

II. The Modified Gysel Power Divider Design Procedure

A. Broad-Band Power Divider Using LGRs

As can be seen in Fig. 1 the primary proposed power divider uses four resistors to obtain a proper power transmission among P_1 and P_2/P_3, and acceptable isolation between P_2 and P_3. In other words S_{12} and S_{13} should be maximized and S_{23} should be minimized in (1), by using LGRs. Also generally S_{ii} should be minimized by impedance matching.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}, \quad (1)$$

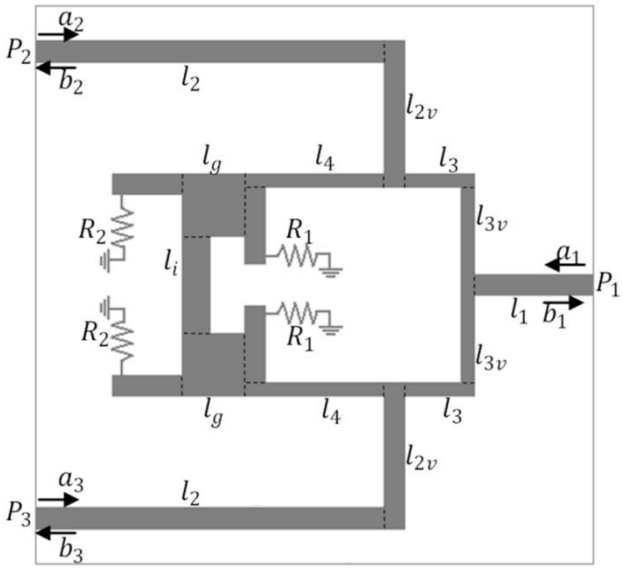
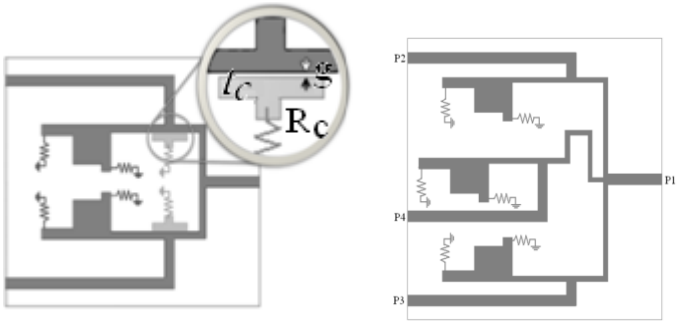


Fig. 1. Primary proposed power divider using four LGRs, the borders of each line is specified with dashed lines.



(a) (b)

Fig. 2. power dividers without connective line, (a) two-way power divider with or without couplers. (b) 3-way power divider. It can easily be generalized to N-way power divider. Paths among input and outputs should be similar.

In the symmetric case, it is desired not to have any current on l_i (connective line), because it increases S_{23} and decreases isolation. By adding LGRs in different structures, this subject will be satisfied for a larger frequency domain. To omit this current, the easiest way is to eliminate l_i, but it causes problems for unbalanced loads, and isolation is not satisfactory in higher frequencies. Adding couplers with LGRs at the end of l_{2v} (as can be seen in Fig. 2 (a)) can be of assistance. But it still has distortions at some frequencies. The dimensions in Fig. 2 (a) are given in Table I and the results are shown in Fig. 3. It is seen that the couplers doesn't have any effect on the scattering parameters of the power divider between 1 GHz and 2.7 GHz, so for the L band power divider the coupled lines are not required. Nevertheless this power divider releases from bounding, cascading or something like that for N-way dividing or combining (N=2, 3, …). The schematic of an L band 3-way power divider is shown in Fig. 2 (b).

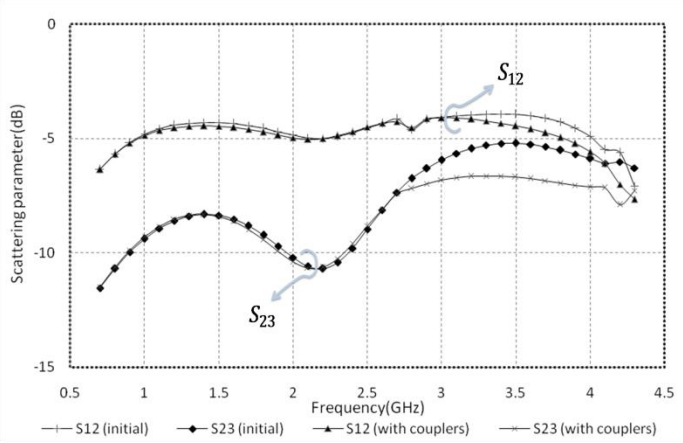


Fig. 3. Comparison between the transmission and isolation of the power dividers without connective lines in Fig. 2 (a).

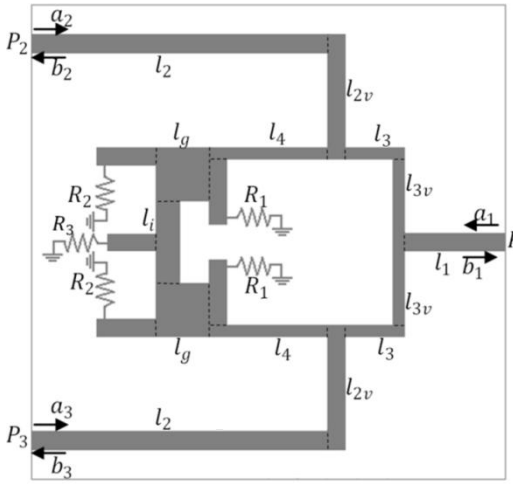


Fig. 4. Power divider using five LGRs.

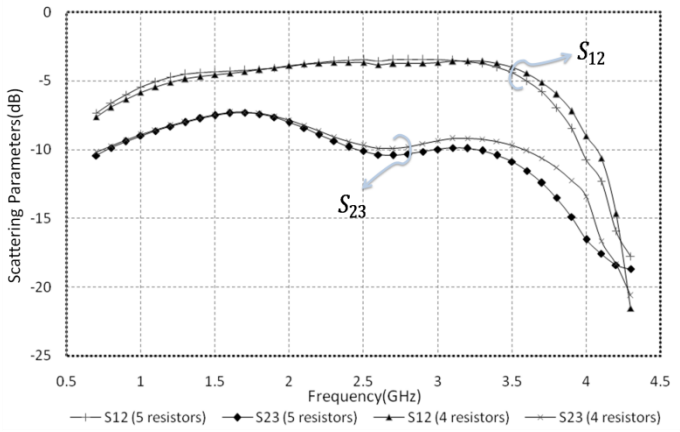


Fig. 5. Comparison between transmission and isolation of 4 and 5 resistors power dividers in Fig. 1 and Fig. 4.

Fig. 4 shows another way for reducing current on l_i, by inserting an LGR at the middle of l_i. As can be seen from Fig. 5, it seems to have a better result. Both of four and five resistors design has the initial values of Table II.

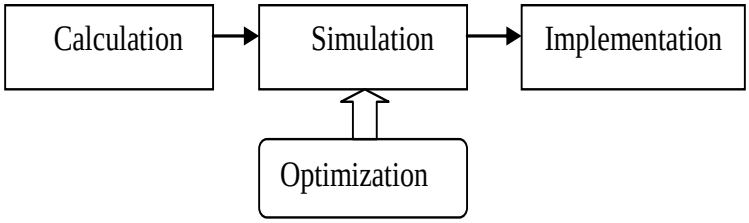


Fig. 6. Phases of the design and optimization.

A. Optimization

Optimization can be used in three phases of the design, calculation, simulation and implementation. In the implementation phase, only limited optimization is available such as changing resistors, and using additional components. But the degrees of freedom in calculation and simulation are more than implementation, and changes can be applied easily to optimize the design. Both of the ways has its advantages and disadvantages. Simulation has more reliable and easy to use results. Calculation may be faster. With advanced and inexpensive processers available, it seems that simulation optimization is better for most designs (Fig. 6).

In this paper Quasi Newton optimizer [16] is used in HFSS [17]. In this method, we have defined (2) as a function from outputs of simulation on each value of n-variables. To obtain acceptable transmission and isolation, S_{12} must be about -3dB, and S_{23} have to be as minimized as possible, we assumed the optimistic destination -50dB. So this function should be minimized.

$$f(x_k) = 5\sum_i \left(dB(S_{12}(\boldsymbol{x_k}))\big|_{fr1_i} + 3\right)^2 + \sum_i \left(dB(S_{23}(\boldsymbol{x_k}))\big|_{fr2_i} + 50\right)^2, \quad (2)$$

x_k is the vector of variables on step k. $fr1_i$ and $fr2_i$ are frequencies and both are the ith component of {1,1.5,…,3.5} GHz. The weighting factor for S_{12} is considered greater than for S_{23} because the minimization of the difference between S_{12} and -3 dB is more important over the minimization of the difference between S_{23} and -50 dB.

The values of components of x_1 (initial values) and x_n (optimized values after n steps for $n = 12$) are available in Table II, and the comparison of initial and optimized results is shown in Fig. 7.

B. Manual Evolutions

The main problem is isolation in low frequencies. So we changed $fr2_i$ in (2) to $fr2_j$ (and its summation operator from i to j) that is the jth component of {1, 1.5, 2} GHz to affect more on low frequencies, and continued the modified optimization for 24 steps. The result is called $x_{12\,24}$ and its values are shown in Table II.

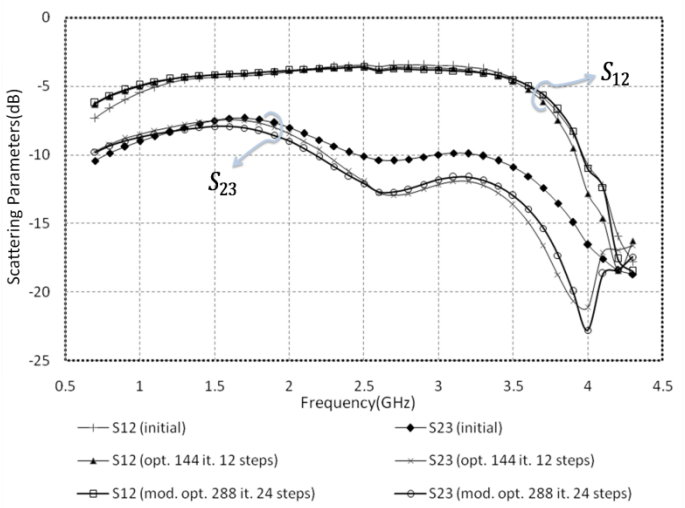


Fig. 7. Isolation and transmission of 5 resistors power divider with initial values, and values after optimization with 144 iterations or 12 steps and also after modified optimization with 288 iterations or 24 steps.

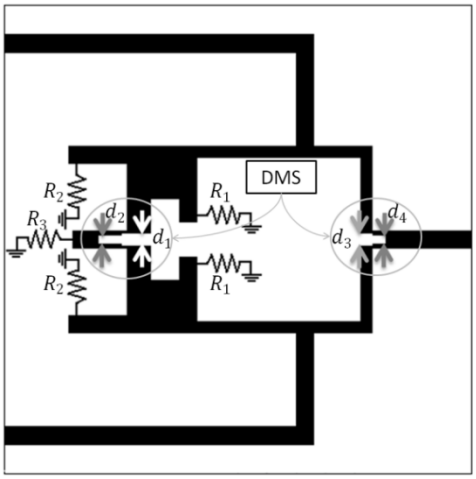


Fig. 8. 5 resistors power divider with DMS. d_is are the names of DMS's rectangles.

For the better isolation, the impedance between the output ports should be increased and for the better transmission the impedance between the input port and the output ports should be decreased. To obtain these together, DMS and also optimized DMS is used as shown in Fig. 8. The DMS can be modeled by inductances and capacitances so that the isolation impedance increases without increasing the transmission impedance. It will be seen further in next section. The DMS's dimensions variable is called y_k instead of x_k and three steps are enough to obtain optimized values. The dimensions values of the DMS are shown in Table III and the results are in Fig. 9.

If we choose deadline of S_{12} to be -5dB (it means 2dB reduction for each port), this power divider will be admitted from 1 to 3.6 GHz.

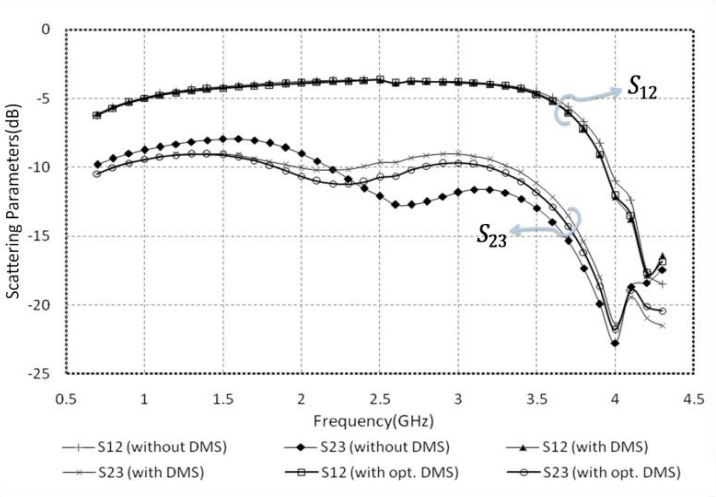


Fig. 9. Isolation and transmission of simulated 5 resistors power divider after modified optimization, with and without optimized DMS.

But this circuit has a problem, and that is impedance matching to 50 Ω (with 10% accuracy). To obtain this impedance, the width of input and output lines should be about 2 mm, using the formula given for narrow line ($w/h < 3.3$) impedance in [18] with the correction coefficient, $k_1 = 5/6$, because of our wave port (this can be different for other wave ports), so the equation will be

$$Z_0 = k_1 \frac{119.9}{\sqrt{2(\epsilon_r + 1)}} \ln\left(4\frac{h}{l_w} + \sqrt{16\left(\frac{h}{l_w}\right)^2 + 2}\right). \quad (3)$$

To meet impedance matching, two limits exist, first the width of input and output lines should be constant (about 2 mm), second the structure of design should not be changed; only Z_{l1} should be same as $Z_{l3}||Z_{l3}$ and Z_{l2} should be same as $Z_{l3}||Z_{l4}$.

To obtain these conditions we scaled down the design, and multiplied its dimensions by $\frac{3.5}{4}$ (excepting z axis or the height of substrate), and kept l_{1_w} and l_{2_w} on their main values. As can be seen in Fig. 11, by the supposed deadline it has acceptable result from 1 to 4 GHz (L and S band), and if we define bandwidth by

$$BW = \frac{1}{2}\left(\frac{fr_{high} - fr_{low}}{fr_{center}}\right) = \frac{fr_{high} - fr_{low}}{fr_{high} + fr_{low}}, \quad (4)$$

it will have 60% bandwidth.

Furthermore, the results can still be improved by using DGS. DGS should also increase the isolation impedance on the ground without increasing the transmission impedance. The shape of DGS is chosen according to Fig. 10, to confine S_{23} and let the LGRs have its currents. The dimensions are obtained by optimization. As implemented in Fig. 11 by using DGS, S_{23} dismounts of -10dB. So by

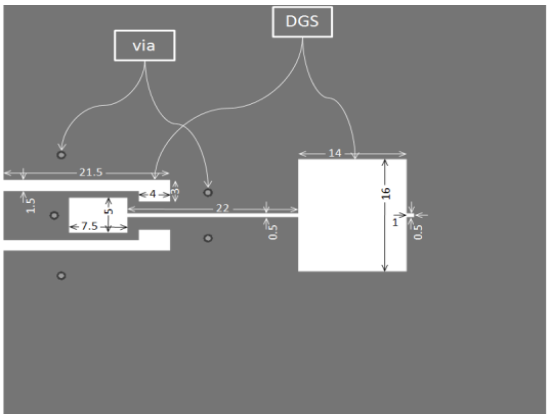


Fig. 10. Location of vias and shape of DGS on ground (dimensions are in millimeter).

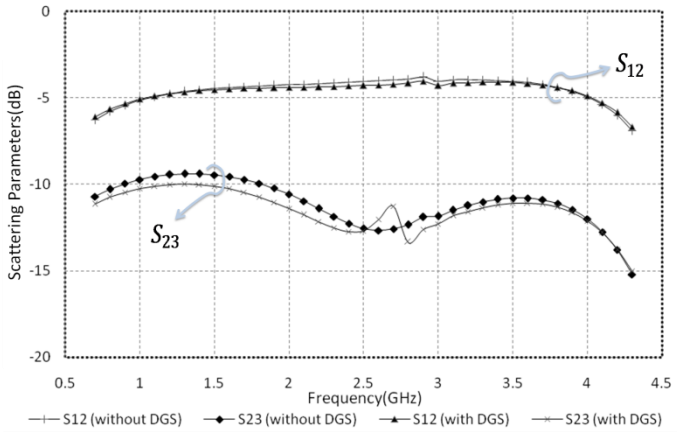


Fig. 11. Simulation results of L&S band power dividers with DMS and impedance matching (with and without DGS).

composition of mathematical optimization and manual evolution the L and S band power divider has been achieved.

III. CIRCUIT MODEL

Up to now the steps of design is declared, but to insure that the design is fully optimized, and the manual evolution doesn't corrupt the initial optimization, a total optimization on the circuit is needed. It can be made using the full circuit model of the design. Also a circuit model can help to detect critical parameters those can increase the efficiency of the design by changing them; which parameters of microstrip should be changed to obtain better results. Circuit preparation for a microstrip design has two main steps, 1) to derive a circuit model for a given design and 2) to find the relations between the microstrip design parameters and the circuit model components.

To obtain a circuit model for a microstrip design with DGS, one way is to see the effect of defected ground on the line of circuit and put the element on the line to model this effect. For example one part of DGS under connective line can be modeled using a capacitor paralleled with an inductor on the line, because as shown in Fig. 12 (a), there are two ways for the current on the ground, one way

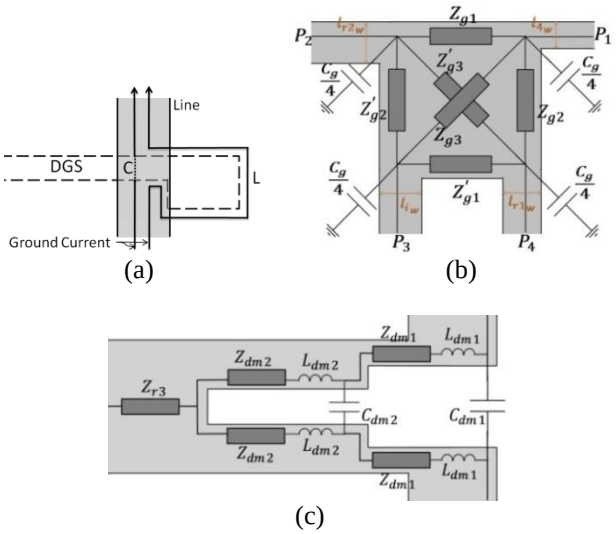


Fig. 12. Deriving circuit model for some parts of the design: (a) Ground currents around the DGS under the connective line, (b) the surface that is called l_g in Fig. 1 and (c) the DMS in Fig. 9 (d_1 and d_2).

is to increase the inductance and the other is to increase the capacitance. The inducting path has longer way for the current, so it should be connected to the line impendence, too. This procedure can be done for all parts of the DGS. By matching the diagrams of simulations and circuit models, the value of each component of the circuit model can be obtained relative to the design's dimensions. Also the DGS's dimensions has an effect on the value of the components of the circuit model for the other parts of the design (e. g. DMS and the microstrip lines those are over the DGS).

As can be seen in Fig. 11, DGS doesn't defect the transmission and isolation results of the power divider without the DGS. Moreover, adding the DGS to the optimized power divider without the DGS, should have better results than adding the DGS to the initial power divider without the DGS. So, if we obtain a full circuit model for the power divider without the DGS and optimize this circuit, and then add the DGS, the results should be same with the optimized circuit with DGS. Therefore the circuit model with complete relations between the dimensions of the design and components of the circuit is derived for the power divider without the DGS, and adding the DGS improved the results. In addition the dimensions of the DGS is derived from the optimization in simulation phase of the design and the circuit model for the optimized DGS added to the power divider's circuit model .

The surface that is called l_g in Fig. 1 is in fact a patch coupler [18] which is a circuit with four ports that increases the capacitance between each of its ports and the ground. The total capacitance can be approximated by four equal capacitance on each ports (as shown in Fig. 12 (b)). To obtain the circuits components due to the physical characteristics of the design, (5) to (12) should be satisfied.

$$l_{g1_l} = l_{g_L} - \left(l_{g2_w} + l'_{g2_w}\right), \tag{5}$$

$$l_{g2_l} = l_{g_w} - \left(l_{4_w} + l'_{g1_w}\right), \tag{6}$$

$$l'_{g1_l} = l_{g_L} - \frac{1}{2}\left(l_{g2_w} + l'_{g2_w} + l_{r1_w} + l_{i_w}\right), \quad (5)$$

$$l'_{g2_l} = l_{g_w} - \frac{1}{2}\left(2l'_{g1_w} + l_{g1_w} + l_{r2_w}\right), \quad (6)$$

$$l_{g1_w} = l'_{g1_w} = 21.85 \tanh^{-1}\left(0.00097 h {l_{g_w}}^{0.83} {l_{g_L}}^{1.17}\right), \quad (7)$$

$$l_{g2_w} = l'_{g2_w} = 21.85 \tanh^{-1}\left(0.00097 h {l_{g_w}}^{1.17} {l_{g_L}}^{0.83}\right), \quad (8)$$

$$l_{g3_w} = 0.44\sqrt{l_{g1_w} l_{g2_w}}, \quad (9)$$

$$l_{g3_l} = \sqrt[4]{\left({l'_{g1_l}}^2 + {l_{g2_l}}^2\right)\left({l_{g1_l}}^2 + {l'_{g2_l}}^2\right)}, \quad (10)$$

$$l_{g3_l} = \sqrt[4]{\left({l_{g1_l}}^2 + {l_{g2_l}}^2\right)\left({l'_{g1_l}}^2 + {l'_{g2_l}}^2\right)}, \quad (11)$$

$$C_g = \epsilon_{eff}\epsilon_0 \sqrt{\frac{10^{-6} l_{g_L} l_{g_w}}{7.58\, h^{0.3} \tan^{-1}\left(\frac{12.1 h^{1.7}}{l_{g_L} l_{g_w}}\right)}}, \quad (12)$$

Where $l_{g_L} = l_{g_l} + l_{r1_w}$ and l_g is defined in Fig. 1 and all the dimensions are in millimeters (here and after). To derive the effective microstrip permittivity, for l_g the relation for $\epsilon_r > 1.3$ should be used from [18],

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + \frac{10h}{\sqrt{l_{g1_l} l_{g2_l}}}\right)^{-0.555}. \quad (13)$$

The above relations are obtain by matching simulations results to circuit modeling results and by using examination of the behavior of the design and the circuit while changing their parameters. This is similar to the conformal mapping approach applied in [19]. The considered limits for these relations are $l_{g_w} l_{g_L} < 400$ and $0.7 < l_{g_w}/l_{g_L} < 1.43$.

The scattering parameters of some examples of this circuit and the similar simulated microstrip circuits are compared in fig. 13.

Fig. 12 (c) shows the proposed circuit model for the DMS in Fig. 9 (d_1 and d_2). The value of C_{dm1} can be obtained using relations as for the Gap capacitance in [18]. By neglecting the even mode capacitance or the line to ground capacitance the result for the line with $0.5 \leq l_{i_w}/h \leq 2$, will be

$$C_{dm1}^{(1)} = \frac{1}{2}\exp\left(4.26 - 1.453 \log\left(\frac{d_{1_w}}{l_{i_w}^{(1)}}\right)\right)\left(\frac{d_{1_w}}{l_{i_w}^{(1)}}\right)^{\frac{l_{i_w}^{(1)}}{h}\left[0.619 \log\left(\frac{l_{i_w}^{(1)}}{h}\right) - 0.3853\right]} \text{ pF}. \quad (14)$$

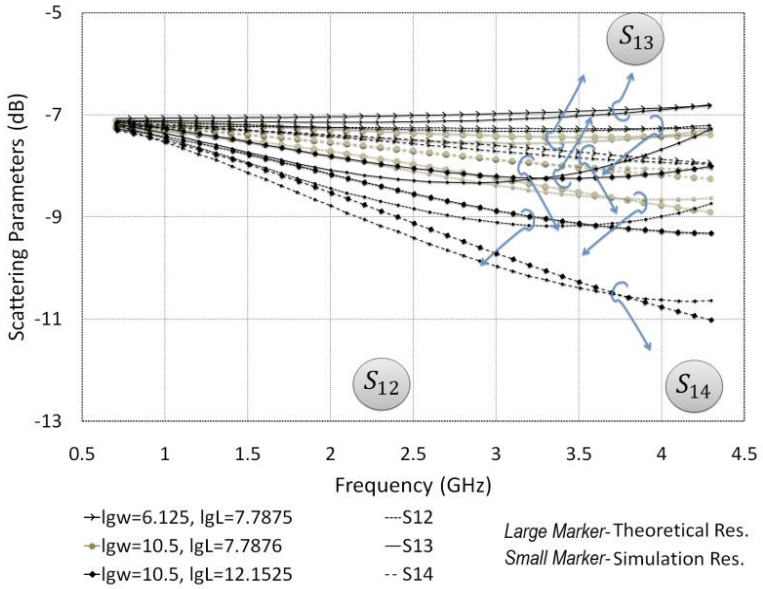


Fig. 13. Examples of the theoretical and the simulation results of the circuit in Fig 12 (b).

For $l_{i_w}/h \geq 2$, C_{dm1} can be estimated by dividing l_{i_w} into N parts and paralleling the capacitances of all parts. N is the integer part of $1 + l_{i_w}/2h$, and

$$C_{dm1} = \sum_{i=1}^{N} C_{dm1}^{(i)}. \tag{15}$$

The second capacitance is C_{dm2}. This is the steps capacitance and for $d_{1_w} > d_{2_w}$ its value is explicitly

$$C_{dm2} = \frac{\epsilon_0}{\pi}\left[\frac{\alpha^2+1}{\alpha}\ln\left(\frac{1+\alpha}{1-\alpha}\right) - 2\ln\left(\frac{4\alpha}{1-\alpha^2}\right)\right] \text{F}, \tag{16}$$

While $= d_{2_w}/d_{1_w}$. L_{dm1} is the bend inductance and with the expression from [18] can be defined,

$$L_{dm1} = 0.1 l_{dm1_l} h\left(4\sqrt{\frac{l_{dm1_w}}{h}} - 4.21\right) \text{nH}. \tag{17}$$

For the steps inductance, L_{dm2}, the general expression in [20] can be exploited,

$$L_{dm2} = 0.4935 h\left(1 - \frac{Z_{dm2}}{Z_{dm1}}\sqrt{\frac{\epsilon_{eff2}}{\epsilon_{eff1}}}\right)^2 \text{nH}. \tag{18}$$

The expressions for Z and ϵ_{eff} can be found in [20] explicitly.

Based on these concepts the total circuit model for the power divider with and without the DGS is given in Fig. 14. This circuit has been optimized and then the DGS added to it. If we add the brightened parts and change some components values over the DGS in the microstrip design, the circuit model for the power divider with DGS will be obtained.

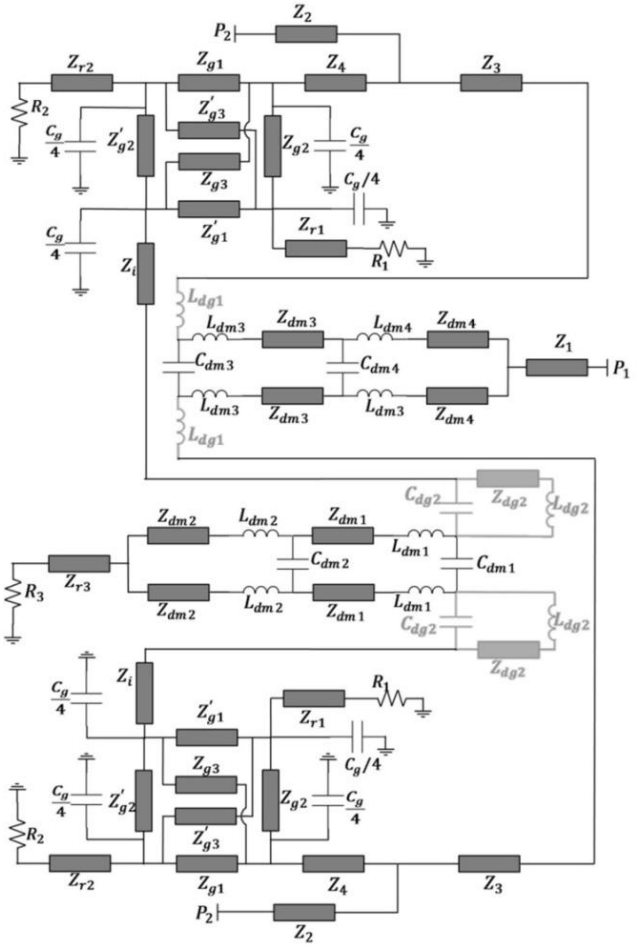


Fig. 14. Complete circuit model for the power divider with and without DGS (The brightened (transparent) parts should be considered as the short circuits).

This circuit can be analyzed and optimized using computer aided design (CAD) tools. The circuit analysis results confirmed the simulation optimization. S_{12} and S_{23} of the optimized circuit those that supersedes the transmission and the isolation of the power divider is shown in Fig. 15. With the proper conventions of the microstrip design, the optimized variables of the microstrip design and the circuit model are approximately the same for the same substrate.

IV. IMPLEMENTATION

Last of all, as shown in Fig. 16 and Fig. 17 by implementing the final design with DMS and DGS, the simulation results are validated and the L&S band power divider with LGRs is fulfilled. The comparison of the results of final simulation and implementation is shown in Fig. 18. Also the phases of S_{12} and S_{21} of implemented design is compared in Fig.18 and it illustrates good phase matching,

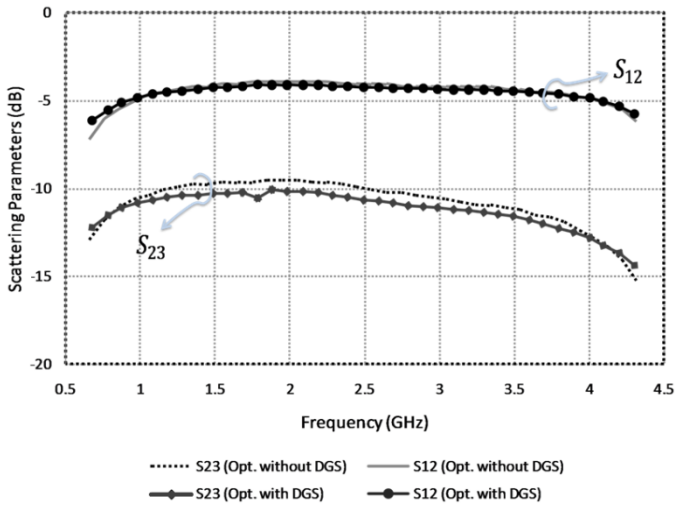


Fig. 15. Isolation and transmission of the optimized circuit model of the power divider without the DGS and the results by adding the effect of the DGS to the circuit.

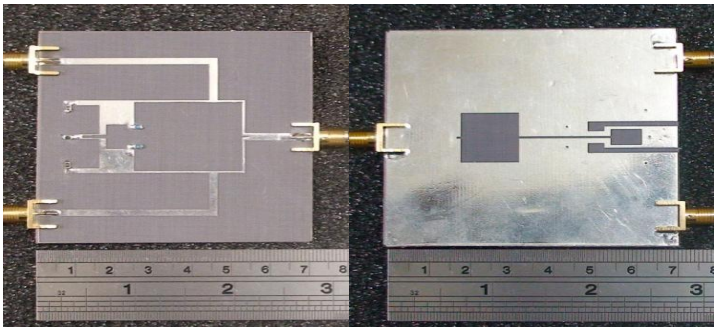


Fig. 16. Photograph of 5 LGRs power divider with DMS and DGS.

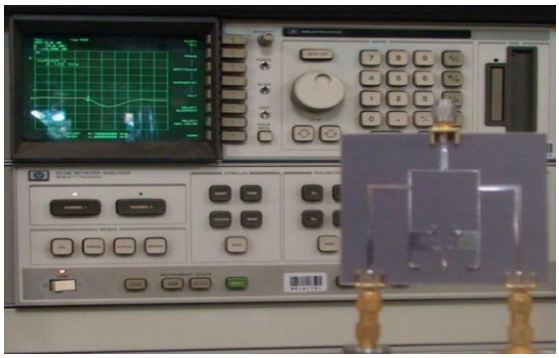


Fig. 17. Testing isolation of the power divider.

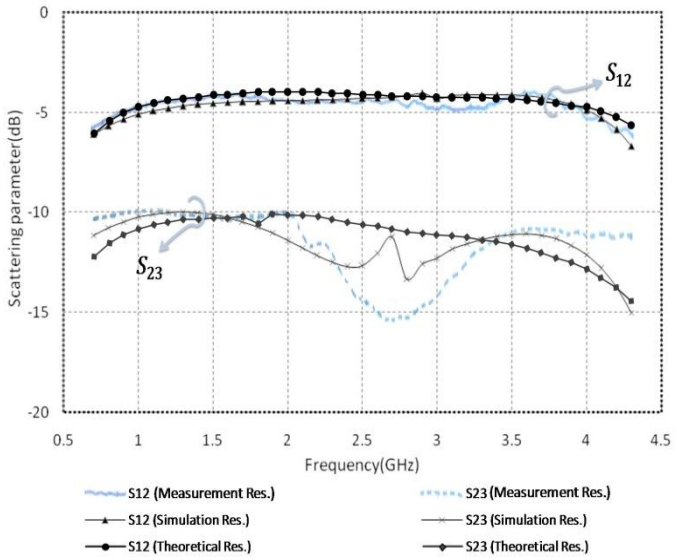


Fig. 18. Isolation and transmission of simulated and implemented final power divider with DMS and DGS.

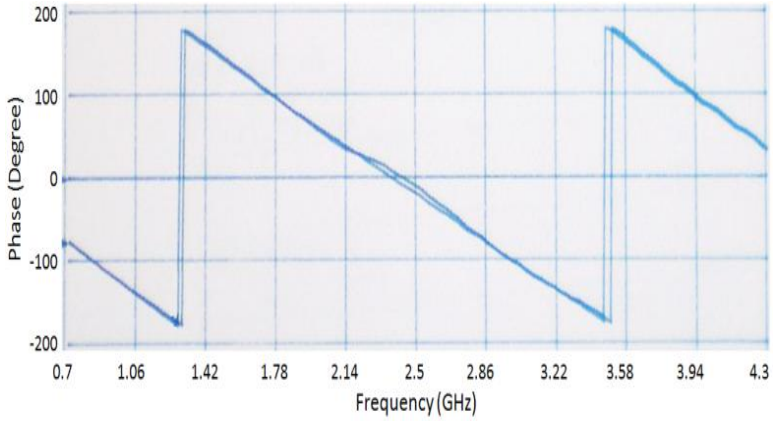


Fig. 19. Measured phases of S_{12} and S_{13} for implemented power divider.

TABLE I: CHARACTERISTICS OF POWER DIVIDER WITHOUT CONNECTIVE LINES.

feature	value	feature	value
ϵ_r	2.55	l_{2v_l}	16mm
$loss\ tangent$	0.001	l_{4_l}	20mm
h	1.27mm	l_{4_w}	2mm
w	7cm	l_{3_l}	10mm
l	8cm	$l_{3_w} = l_{3v_w}$	2mm
l_{2_l}	5cm	l_{g_l}	9mm
l_{1_w}	3mm	l_{g_w}	10mm
$l_{2(v)_w} = l_{1_w}$	3mm	g	0.3mm
d	5mm	R_1	17 Ω
l_{c_l}	8mm	R_2	17 Ω
l_{c_w}	2mm	R_c	33 Ω

TABLE II: X_K'S COMPONENTS VALUES FOR INITIAL, OPTIMIZED AND MODIFIED OPTIMIZED CASES.

Constant values $\epsilon_r = 2.55, loss\ tangent = 0.001, h = 0.762mm,\quad w = l = 8cm, l_{2_l} = 5cm,$ $l_{2_w} = l_{2v_w} = l_{1_w} = 1.9mm, d = 1cm$			
x_k Components Name	x_1 Components Values (Initial)	x_{12} Components Values (Optimized)	$x_{12\,24}$ Components Values (Modified Optimized)
l_{2v_l}	16.3mm	17.01mm	17mm
l_{4_l}	22mm	23.9mm	23.89mm
l_{4_w}	1.3mm	0.98mm	0.85mm
l_{3_l}	10mm	7.9mm	7.95mm
$l_{3_w} = l_{3v_w}$	1.3mm	۰.98mm	0.85mm
l_{g_l}	8mm	8.35mm	8.3mm
l_{g_w}	8mm	9.32mm	9.28mm
l_{i_w}	3mm	2.25mm	1.97mm
R_1	31.5 Ω	25 Ω	25(24.9) Ω
R_2	31.5 Ω	24 Ω	24 Ω
R_3	31.5 Ω	45 Ω	45(47) Ω

TABLE III: DIMENSION VALUES OF DMS AND OPTIMIZED DMS.

y_k Components Name	y_0 Components Values (Initial)	y_3 Components Values (Optimized)
d_{1_l}	4mm	4mm
d_{1_w}	1.5mm	1.21mm
d_{2_l}	4mm	3mm
d_{2_w}	1mm	0.81mm
d_{3_l}	1mm	1.08mm
d_{3_w}	0.2mm	0.3mm
d_{4_l}	1mm	1.03mm
d_{4_w}	0.2mm	0.2mm

V. CONCLUSION

A novel Gysel power divider with two octave bandwidth is simulated and fabricated, using regular optimization and manually modified optimization, DMS, impedance matching, and DGS. The advantages of the design are: It has wide bandwidth, simple structure, it is inexpensive and it can be known as a compacted circuit, using a substrate with higher permittivity. Therefore, only regular and mathematical operations and only manual restructuring doesn't lead to the best results, but using both of them on its position is needed. By this method we obtained the widest bandwidth for power

dividers those work with LGRs, up to now. It has the transmission and isolation bandwidth of 60% as defined in the paper and 120% by the definition of the references.

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