Analysis and design of a CMOS current reused cascaded distributed amplifier with optimum noise performance

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***Abstract*- In this paper, analysis, simulation and design of a distributed amplifier (DA) with 0.13µm CMOS technology in the frequency range of 3-40 GHz is presented. Gain cell is a current reused circuit which is optimum in gain, noise figure, bandwidth and also power dissipation. To improve the noise performance in the frequency range of interest, a T-matching low pass filter LC network is utilized at the input gate of the designed amplifier. By this means, the proposed cascaded DA shows about 28% improvements in noise figure and 20% improvement in the gain compared with those of the other well-known configuration. To show the capability of the proposed method we also compared the figure of merit of the proposed amplifier with those obtained with the other researches and showed that this figure is around 38% higher than that of those achieved by other researchers. The figure of merit includes gain, bandwidth, power consumption and also noise figure.**

***Index Terms*-** Distributed amplifier (DA), current reused structure, Conventional distributed amplifier (CDA), Cascaded single stage distributed amplifier (CSSDA), Figure of merit (FOM).

I. INTRODUCTION

Broadband amplifiers have been widley used in many systems such as, electronic warfare, microwave imaging and also optical tranceivers. In order to realize a broadband amplifier, Conventional Distributed Amplifiers (CDAs) are a good candidate due to thier ultra-wide band properties [1]. In [2], a GaAs hybrid and MMIC technologies have been introduced. Due to low cost and integration ability of distributed amplifiers (DAs), these amplifiers were also used in CMOS technology [3].

However, due to the additive gain mechanism of DA, this amplifier is not suitable in applications which high gain is required. This disadvantage of DA (low gain property) is more serios in CMOS technology due to the low transconductance and high substrate loss in a silicon-based process. In order to take the full advantage of the multiplicative gain mechanism of DA, two-dimensional DAs,

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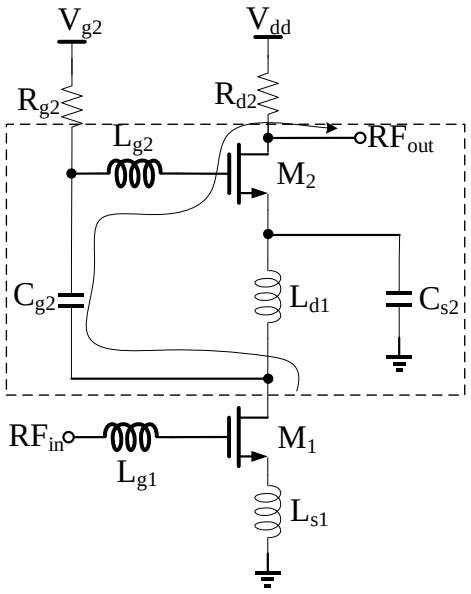


Fig. 1. Gain cell with the current reused structure

such as cascaded multi-stage distributed amplifier (CMSDA) [4] and matrix DA [5], have been proposed. However, in most cascaded DA topologies, the number of cascaded stages is typically smaller than that of the distributed cells, making the gain primarily determined by the additive mechanism instead of the multiplicative one. Hence, CSSDA has been proposed to take full advantage of the multiplicative gain mechanism [6]. Although the CSSDA has potential of higher gain bandwidth performance than that of other DA topologies, its output power is limited by the device size of the last stage. A larger aspect ratio of transistor results in higher output power at the cost of a degraded bandwidth. To improve the performance of the CSSDA, a DA with cascaded gain stages was proposed to achieve higher output power without sacrificing the bandwidth [7]. In addition to the gain-bandwidth performance, power dissipation was another parameter which should be considered. For this purpose, gain cell based on current reuse was proposed [8]. This configuration simply has the power dissipation of one stage but the power gain amplitude of two stages.The prospective of this paper is as follow. In the second section, the current reused circuit is analyzed. Then source degeneration inductance and gate matching network are added and the analysis and design of the circuit is done. In the third section simulation results of the three stages cascaded distributed amplifier are presented and compared with those of the other reported amplifiers. Finally, in the fourth section, the paper is concluded.

II. ANALYSIS AND DESIGN OF DISTRIBUTED AMPLIFIER WITH CURRENT REUSED CELL

Fig. 1 shows the structure of the current reused amplifier. This circuits is fully analyzed in [9]. Two of the main aspects of this configuration are: low power consumption and high power gain. In the first stage of this circuit, a trade-off exists between noise and linearity. In order to moderate this compromise, the noise impedance is calculated and optimized by utilizing a proper matching network

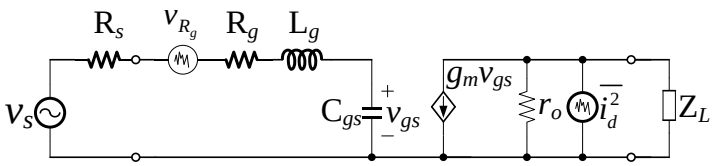


Fig. 2. Small signal model of the common source structure without source degeneration inductance

at the input. Small signal model of the first stage of the current reused circuit is showed in *Fig. 2*. Noise sources are $\overline{v_s^2} = 4kT\Delta f R_s$ for source resistance, $\overline{v_g^2} = 4kT\Delta f R_g$ for gate resistance, and $\overline{i_d^2} = 4kT\Delta f \frac{\gamma}{\alpha} g_m$ for transistor channel. In this analysis, the gate noise is neglected (this assumption is held for the frequencies well below than cutoff frequency). Suppose that $R_s >> R_g$, therefore noise factor is derived as follows:

$$F = 1 + \frac{R_g}{R_s} + (\frac{\gamma}{\alpha})(\frac{\omega}{\omega_T})^2 g_m R_s \tag{1}$$

The optimum noise impedance is obtained by equating the derivation of the noise factor with respect to R_s given in (1) to zero. This optimum noise impedance is derived as follows:

$$R_{s,opt} = (\frac{\omega_T}{\omega}) \sqrt{\frac{R_g}{(\frac{\gamma}{\alpha}) g_m}} \tag{2}$$

Substituting (2) into (1), the minimum noise factor is:

$$F_{\min} = 1 + (\frac{\omega}{\omega_T}) \sqrt{g_m R_g \frac{\gamma}{\alpha}} \tag{3}$$

The following assumptions are held to calculate a predesign value for $R_{s,opt}$: $f_T = 90\ GHz$, $f = 35\ GHz$, $\frac{\gamma}{\alpha} = 1.25$, $g_m = 25\ mS$, $R_g \approx \frac{1}{5g_m} = 8\ \Omega$. Thus, the optimum value of the noise resistance using (2) is $R_{s,opt} \approx 40\ \Omega$ and therefore the minimum noise factor of the first stage of the current reused circuit is $NF_{\min} = 1.2$ or $NF_{\min} = 10\log F_{\min} = 0.8\ dB$.

Input impedance of the circuit shown in *Fig. 1* is expressed as:

$$Z_{in} = R_g + \frac{g_m L_s}{C_{gs}} + j[\omega(L_g + L_s) - \frac{1}{\omega C_{gs}}] \tag{4}$$

The first term in (4) is the result of source inductance feedback. The source inductance introduces the real part for input impedance and can be used for input impedance or noise matching. Now the source impedance can be calculated for minimum noise figure as follow:

$$\mathrm{Re}(Z_{in}) = R_g + \frac{g_m L_s}{C_{gs}} = R_g + \omega_T L_s = R_{opt} \rightarrow L_s = \frac{R_{opt} - R_g}{\omega_T} \tag{5}$$

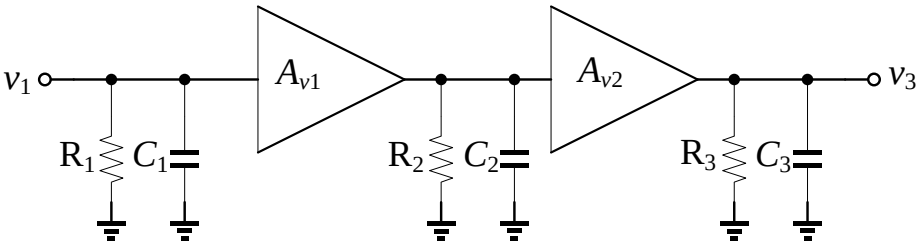
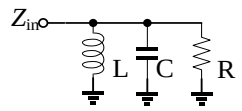
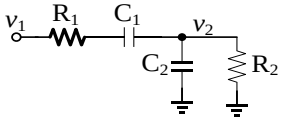
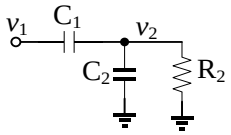
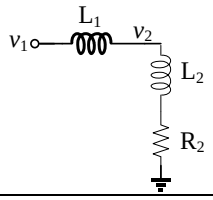


Fig. 3. Two stage of ideal amplifiers with nodal resistance and capacitance

Table I. Pole and zero of some of the rlc circuit configurations

			
$\omega_{p1} \cong -\frac{1}{RC}$ $\omega_{p2} = -\frac{R}{L}$	$\omega_{p1} = -\frac{1}{R_1 C_1}$ $\omega_{p2} = -\frac{1}{R_2 C_2}$	$\omega_p = -\frac{1}{R_2(C_1 + C_2)}$	$\omega_p = -\frac{R_2}{L_1 + L_2}$
-	$\omega_z = 0$	$\omega_z = 0$	$\omega_z = -\frac{R_2}{L_2}$

However the gate resonant frequency is obtained by equating the imaginary part of (4) to the zero. Therefore the gate resonant frequency is:

$$\omega_0 = \frac{1}{\sqrt{C_{gs}(L_g + L_s)}} \tag{6}$$

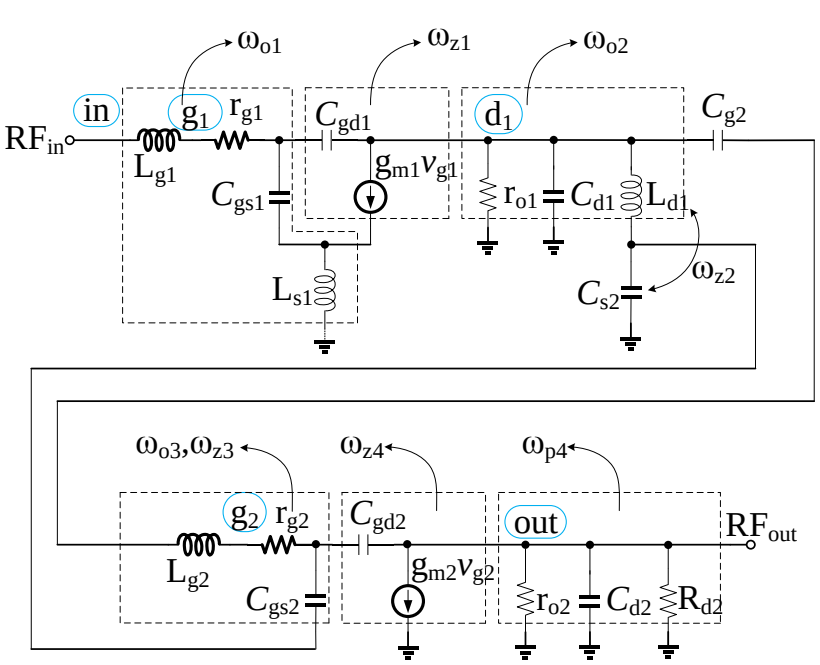
The above method is only valid for narrowband application since the noise matching is only achieved at the resonance frequency of gate $\omega_0 = \frac{1}{\sqrt{C_{gs}(L_g + L_s)}}$ where the input impedance given by (4) is a purely real.

III. DESIGN OF CURRENT REUSED CIRCUIT WITH SOURCE DEGENERATION INDUCTOR

In order to derive a transfer function for a circuit, the following method is used in this paper. Assuming a two stage amplifier with ideal gain cells, as shown in *Fig. 3*. Resistance and capacitance of each node is extracted. The transfer function for this circuit can be expressed as:

$$\frac{v_3}{v_1} \cong A_{v1} \times A_{v2} \times \frac{1}{1+\frac{s}{s_{p1}}} \times \frac{1}{1+\frac{s}{s_{p2}}} \times \frac{1}{1+\frac{s}{s_{p3}}};\ \ s_{pi} = \frac{1}{R_i C_i} \tag{7}$$

Resistance and capacitance of each node generate a pole at that node. A_{v1} and A_{v2} are the low frequency gains of gain cells. This method is very simple and accurate enough. Other circuit



$$\omega_{o1} \approx \frac{1}{\sqrt{(L_{g1}+L_{s1})C_{gs1}}}$$

$$\omega_{o2} \approx \frac{1}{\sqrt{L_{d1}C_{d1}}}$$

$$\omega_{o3} \approx \frac{1}{\sqrt{L_{g2}C_{gs2}}}$$

$$\omega_{p4} \approx -\frac{1}{(r_{o2} \parallel R_{d2})C_{d2}}$$

$$\omega_{z1} \approx \frac{g_{m1}}{C_{gd1}}$$

$$\omega_{z2} \approx \frac{1}{\sqrt{L_{d1}C_{s2}}}$$

$$\omega_{z3} = 0 \qquad \omega_{z4} \approx \frac{g_{m2}}{C_{gd2}}$$

Fig. 4. Small signal model for the circuit of *Fig. 1*

configurations are depicted in Table I. As an example, parallel RLC circuit generates two poles at: $\omega_{p1} = -\frac{1}{RC}$ and $\omega_{p2} = \frac{L}{R}$. Transfer function of the proposed circuit is derived using the described simple method and Table I.

Small signal model of the two stages cascaded circuit of *Fig. 1* is depicted in *Fig. 4*. As can be seen, the poles and zeros are determined in term of the circuit elements. These poles and zeros are calculated implementing a proper circuit simplification. Resonance frequencies ω_{01} and ω_{03} should be placed at the higher frequency band of 35 GHz. It should be noted that the gate-source capacitance of both transistors M_1 and M_2 are lower than 100 *f*F. On the other hand, for M_1 with $g_m = 25\,mS$, $I_{ds} = 4\,mA$, and the cutoff frequency of 95 GHz, the source inductance using Eq. (5) is $L_{s1} = \frac{R_{in}}{\omega_T} = 62\,pH$. The value of C_{gs1} and C_{gs2} are 44 *f*F. Therefore, the value of gate inductance of M_1, i.e. L_{g1}, using (6) with $\omega_0 = 2\pi \times 35$ GHz is 512 pH. The same procedure can be used to calculate the gate inductance of M_2, i.e. L_{g2}, which is obtained to be 0.6 nH. ω_{02}, ω_{p4}, ω_{z1}, and ω_{z4} are higher than the higher end of frequency band while zeros ω_{z2} and ω_{z3} are lower than the lower end of the frequency band. Since there is a conjugate pole near the lower end of the frequency band, zeros ω_{z2} and ω_{z3} flatten the slope of the signal in band.

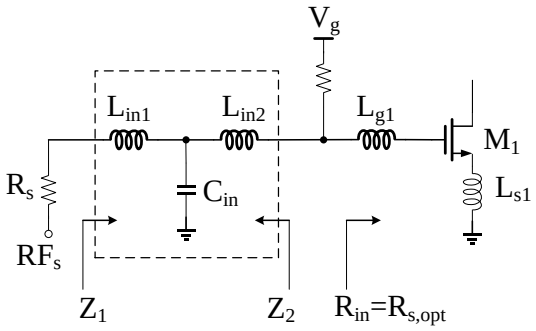


Fig. 5. Matching network circuit

IV. DESIGN OF T-MATCHING NETWORK AT THE INPUT IN ORDER TO IMPROVE CIRCUIT PERFORMANCE

Circuit of *Fig. 1* needs a matching network at the input to match 40 Ω optimum noise resistance to 50 Ω source resistance. The proposed matching network is presented with series *L* and parallel *C* as in *Fig. 5*. In this figure, impedances Z_1 is expressed as follows:

$$\begin{aligned} Z_1 &= sL_{in1} + \frac{1}{sC_{in} + \dfrac{1}{sL_{in2} + R_{in}}} = sL_{in1} + \frac{sL_{in2} + R_{in}}{sC_{in}\left(sL_{in2} + R_{in}\right) + 1} \\ &= sL_{in1} + \frac{1}{L_{in2}C_{in}} . \frac{sL_{in2} + R_{in}}{s^2 + \dfrac{R_{in}}{L_{in2}} s + \dfrac{1}{L_{in2}C_{in}}} . \end{aligned} \tag{8}$$

At the resonance frequency of $\omega_2 = 1/\sqrt{L_{in2}C_{in}}$ the last expression is simplified as follow:

$$Z_1 = sL_{in1} + \frac{L_{in2}}{C_{in}R_{in}} + \frac{1}{sC_{in}} \tag{9}$$

For a complete input impedance matching, Z_1 should be matched to R_s. Therefore, we have:

$$sL_{in1} + \frac{L_{in2}}{C_{in}R_{in}} + \frac{1}{sC_{in}} = R_s .$$

Similarly, it could be stated that at the resonance frequency of $\omega_1 = 1/\sqrt{L_{in1}C_{in}}$, Z_2 can be expressed as:

$$Z_2 = sL_{in2} + \frac{L_{in1}}{C_{in}R_s} + \frac{1}{sC_{in}} \tag{10}$$

Z_2 should be matched to R_{in} , and:

$$sL_{in2} + \frac{L_{in1}}{C_{in}R_s} + \frac{1}{sC_{in}} = R_{in} . \tag{11}$$

Proposed matching network is a low pass filter and two resonance frequencies are $\omega_1 = 1/\sqrt{L_{in1}C_{in}}$ and $\omega_2 = 1/\sqrt{L_{in2}C_{in}}$. If both resonance frequencies are equal to $2\pi \times 35\ (Grad/s)$ and $L_{in1} = L_{in2}$, then the

Table II. Simulation results of common source, simple current reused, and improved current reused distributed amplifiers

Structure	**BW (GHz)**	**P_{DC} (mW)**	**S_{21} , avg (dB)**	**S_{11} , avg (dB)**	**S_{22} , avg (dB)**	**NF (dB)**	**FOM**
Common source	40	104	17	-12	-9	3.3-6.7	1.98
Simple current reused	35	46	20	-25	-22	7.8-9.2	1.95
Improved (proposed) current reused	37	60	24	-10	-20	5.6-8	2.70

value of capacitance and inductance of matching network are 102 *f*F and 203 pH respectively.

V. THE SIMULATION OF THE CASCADED DISTRIBUTED AMPLIFIER WITH IMPROVED CURRENT REUSED GAIN CELL

The final structures of the proposed distributed amplifier with improved current reused gain cell are showed in *Fig. 6* through *Fig. 8.* Simulations are done with Advanced Design System (ADS) from Agilent and circuit element models are from TSMC foundry. Circuit elements are from 130 nm RF CMOS general purpose technology. The number of the cascaded stages of three gives the best results. Results of common source, simple current reused, and improved current reused (*Fig. 6*) gain cells distributed amplifiers are depicted in *Fig. 10* and *Fig. 10* for comparison. In this figure, curves with no symbol, square symbol, and circle symbols are related to common source, simple current reused, and improved current reused circuits respectively. S_{21} of improved circuit is more flat than two other circuits. Bandwidth of improved circuit is about 0.5 GHz wider than simple circuit. S_{11} which represents the input matching, in improved circuit is better than simple circuit in the high corner of the bandwidth. It is mainly because of using matching circuit of *Fig. 5* at the input of the amplifier. The matching circuit *Fig. 5* is designed to work at higher frequencies near 40 GHz. As a result better gain and input matching is achieved at these high frequencies. It is also worth to mention that noise figure of proposed amplifier in high frequencies near 40 GHz is improved respect to the simple current reused circuit. This is also due to proper noise matching at the input stage. Noise figure of the common source amplifier is better than simple current reused and improved current reused circuit. This is due to the numerous number of on-chip inductors used in current reused circuit. This inductors are usually made with low quality and therefore produce high noise at high frequencies. Noise figure of the current reused circuit at low frequencies (frequencies lower than 1 GHz) is very high since current reused circuit blocks signals with low frequency; hence no power gain is achievable in low frequencies.

Figure of merit given by (10) is used for comparison.

$$FOM = \frac{S_{21}(dB).BW(GHz)}{P_{DC}(mW).NF(dB)} \qquad (12)$$

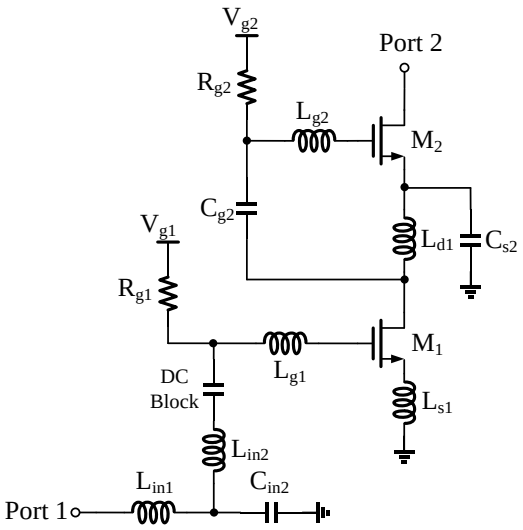


Fig. 6. Final structure of the improved current reused gain cell

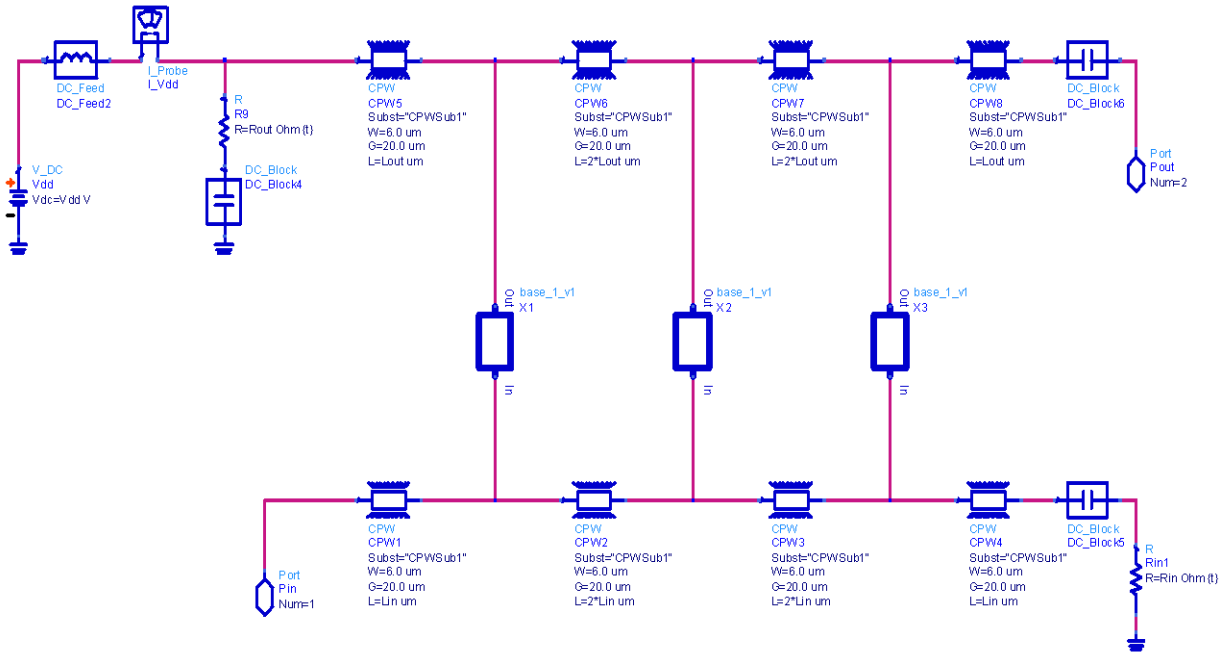


Fig. 7. Final structure of the distributed amplifier with three improved current reused gain cell stages

As can be seen in Table II, the noise performance of the proposed circuit is 28% lower than that of common source circuit and its minimum is 5.6 dB. Bandwidth of the proposed circuit is about 6% wider than that of common source and is 37 GHz. The gain of the proposed amplifier is also 20% higher than that of simple current reused amplifier. The amplifier has also FOM of 2.7 which is about 38% higher than those of two other circuits. Finally, in Table III the comparison is made with the results reported by other references.

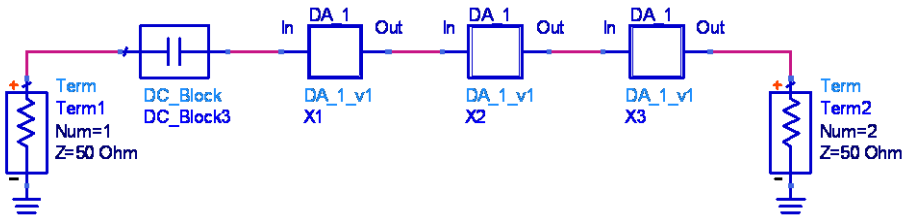
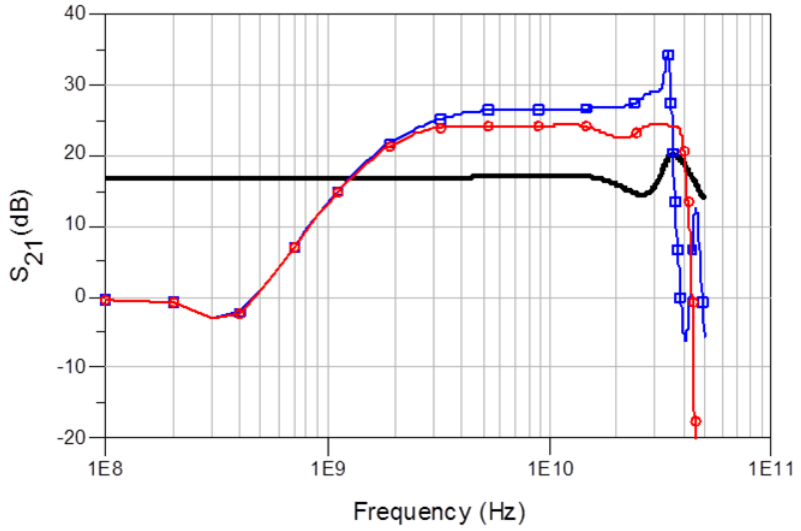


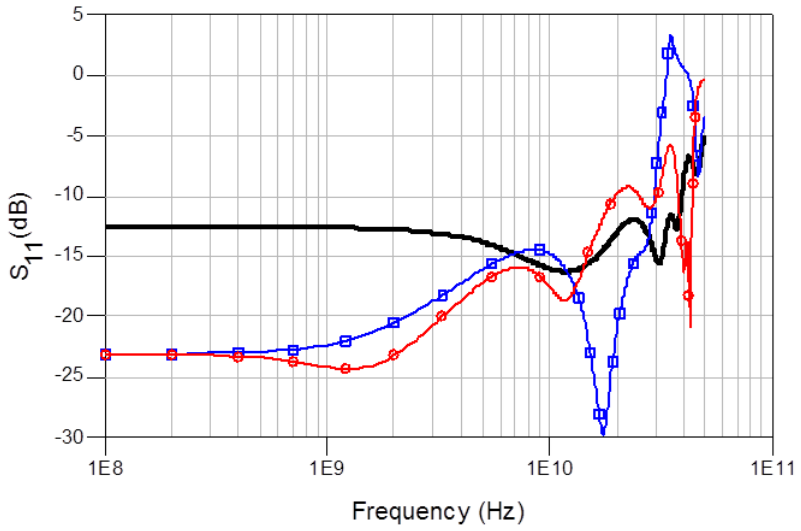
Fig. 8. Final structure of the proposed cascaded distributed amplifier in three stages

Eqn Pdc_1=-3*1.2*X1.Vdd.i Eqn Pdc_2=-3*1.2*MDA_2..X1.Vdd.i Eqn Pdc_3=-3*1.2*MDA_3..X1.Vdd.i

freq	Pdc_1	Pdc_2	Pdc_3
0.0000 Hz	0.104	0.060	0.060

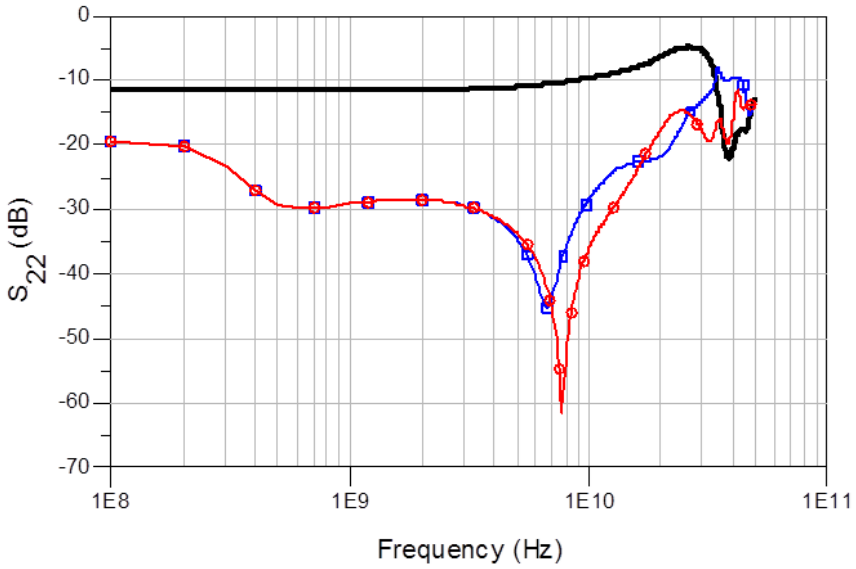


(a)

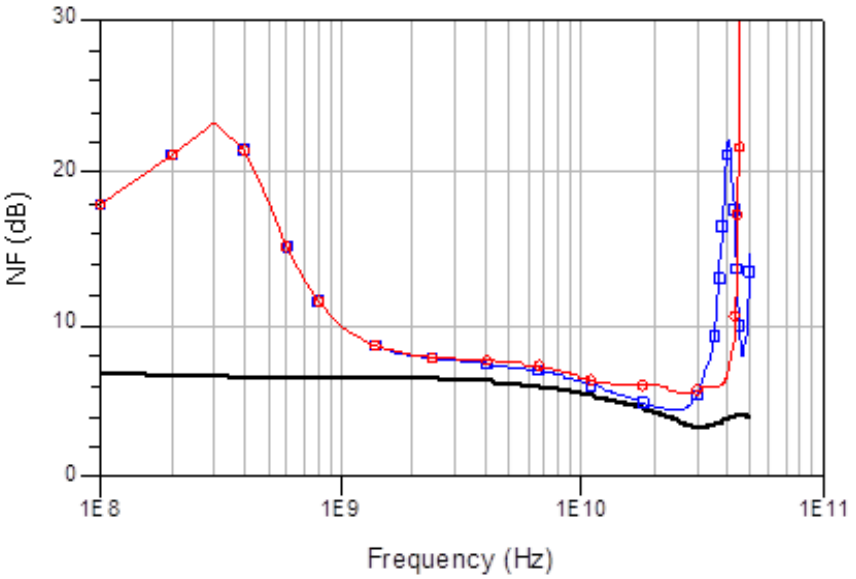


(b)

Fig. 9. (a) Power gain (S_{21}) and (b) input return loss (S_{11}) of the three stage cascaded distributed amplifiers with common source (no symbol and black color), simple current reused (with square symbol and blue color), and improved current reused (with circle symbols and red color) core circuits. Hint: power consumption of the three blocks of each cascaded DA with 1.2 V power supply is reported above the figure (a); Pdc_1, Pdc_2, and Pdc_3 are for "common source", "simple current reused", and "improved (proposed) current reused" DAs respectively.



(a)



(b)

Fig. 10. (a) Output return loss (S_{22}) and (b) noise figure (NF) of the three stage cascaded distributed amplifiers with common source (no symbol and black color), simple current reused (with square symbol and blue color), and improved current reused (with circle symbols and red color) core circuits

VI. CONCLUSION

In this paper, a common source gain cell was first investigated. Then a method was implemented to simultaneously optimize the noise and impedance performances. Consequently, the improved gain cell with source degeneration, current reused and input matching network were proposed to design a CCSDA. Final results showed that the method proposed in this paper successfully improve amplifier performances including power dissipation, noise, gain and the figure of merit.

Table III. Results of some reported das and the proposed da for comparison

Ref.	**Year**	**Tech.**	**BW (GHz)**	**S_{21} avg**	**Voltage-Power**	**NF_{min}**	**FOM**
[10]	2004	180 nm CMOS	DC-22	7.3	1.2-52	3.4	0.91
[4]	2009	90 nm CMOS	DC- 73.5	14	1.2-84	-	-
[11]	2012	65 nm CMOS	DC-65	22	na1-97	6.9	2.14
[12]	2013	65 nm CMOS	2.1-39	10	na-25.5	4.5	3.40
[13]	2013	90 nm CMOS	DC-61.3	7	2.2-60	4.1	1.74
[14]	2013	180 nm CMOS	DC-33	24	2.8-238	6.5	0.51
This work	2014	130 nm CMOS	3-40	24	1.2-60	5.6	2.64

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