Design, Analysis and Simulation of a Linear Phase Distributed Amplifier

Hossein Ghani and Mahmoud Mohammad-Taheri
School of Electrical and Computer Engineering, Faculty of Engineering, University of Tehran, Tehran, Iran,
hosein.ghani@ut.ac.ir, mtaheri@ut.ac.ir
Corresponding author: Mahmoud Mohammad-Taheri

***Abstract*- In this paper a new method for the design of a linear phase distributed amplifier in 180nm CMOS technology is presented. The method is based on analogy between transversal filters and distributed amplifiers topologies. In the proposed method the linearity of the phase at frequency range of 0-50 GHz is obtained by using proper weighting factors for each gain stage in cascaded amplifier topology. These weighting factors have been extracted using MATLAB software. Finally, by plotting the frequency response of the amplifier resulted from MATLAB code and also simulation from ADS, the phase linearity of the designed amplifier is shown.**

***Index Terms*-** Distributed Amplifier; Group delay; Transversal Filter; Linear phase; Weighting

I. INTRODUCTION

In the design of optical receiver, the phase linearity of the pre-amplifier is a main requirement in order to avoid intersymbol interference. Amplifiers used in these receivers should be also wideband. Considering these two main requirements, the distributed amplifiers could be a good candidate as the bandwidth of these amplifiers is theoretically infinite if one does not take into account the transmission line loss. In order to use a distributed amplifier (DA) as a linear phase amplifier we should find an analogy between DA and a transversal filer which has linear phase frequency response. Jutzi [1] was the first researcher which used the DA as a transversal filter at low microwave frequencies. In general, the implementation of distributed amplifiers in solid-state technologies such as GaAs [2], SiGe [3] will result in a very wideband amplifier. However due to integrability, cost and intrinsic speed, the CMOS technology is a good candidate for realization of distributed amplifiers [4-

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6]. In this paper we first considered the technique used in [7] for linearization of the distributed amplifier. In [7], using the analogy between distributed amplifier and transversal filter, a linear phase distributed amplifier was designed and simulated in the frequency range of 0-40 GHz in P-HEMT technology. However due to above mentioned advantages of CMOS technology, in this paper we used this technology for design and analysis of linear phase distributed amplifier. It is worth mentioning that due to large values of parasitic capacitors in CMOS technology, we cannot implement the method used in [7]. Therefore, in this paper, we designed a cascaded multi-stage amplifier and used the proper weighting factors for gains and delays of each transistor to obtain the desired phase response. In section 2, a topology of a conventional distributed amplifier is introduced. In section 3, the analyzed topology in [7] is briefly discussed. Finally in section 4, our proposed topology is introduced and analyzed. In section 5, the results obtained by our proposed method are presented.

II. CONVENTIONAL DISTRIBUTED AMPLIFIER TOPOLOGY

Fig. 1 shows a block diagram of a conventional distributed amplifier. In this amplifier, the parasitic capacitors of transistors have been absorbed into gate and drain inductors to realize an artificial gate and drain transmission lines. In ideal case, the gate inductor (L_g) and parasitic gate-source capacitor (C_{gs}) construct an artificial gate transmission line. (In the case of using a transmission line in gate circuit instead of an inductor, the gate-source capacitor will be in parallel with transmission line capacitor). The same is true for drain circuit. It means the drain-source capacitor (C_{ds}) will construct an artificial transmission line with drain inductor (L_d). Therefore the parasitic capacitors of the transistor will be absorbed into gate and drain transmission lines and this increase the bandwidth of distributed amplifier (as the bandwidth of lossless transmission line is infinite). In conventional distributed amplifier, the input signal will propagate in gate line (input line) and each transistor will receive part of input signal and the amplified signal will be injected into drain line (output line). The end part of gate and drain lines are terminated by Z_g and Z_d respectively to absorb the undesired reflected signals. The input voltage to the gate line is amplified by each transistor and introduced current in the drain terminal. In order to have a strong output signal, the signals travel in drain line in the right direction should be in phase while the signals travel in the left side in the drain line (backward signals) should be out of phase and absorbed into Z_d.

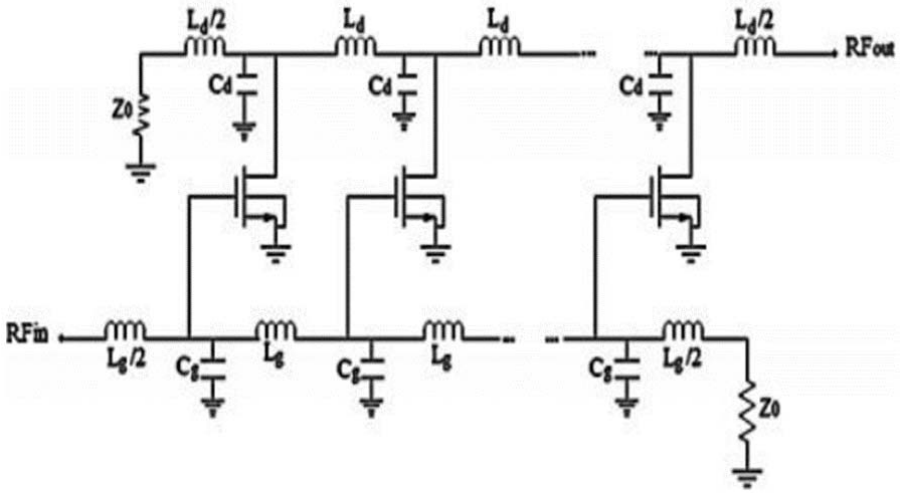


Fig. 1. Conventional Distributed Amplifier

III. LINEAR PHASE AMPLIFIER TOPOLOGY USING TRANSVERSAL FILTER CONCEPT [7]

Block diagram of a transversal filter is shown in Fig. 2. The delay lines were realized by piece of transmission lines which are presented by inductors. The final output is obtained by summing the sampled signals which are multiplied by gain $G_1, G_2, \ldots, G_N$.

To realize the DA topology, each delay line should be replaced by a piece of transmission line and each gain parameter should be presented by a transistor gain. The topology of linear phase distributed amplifier which is analogy to the transversal filter is shown in Fig. 3. The voltage transfer function of the circuit shown in Fig. 2 can be easily derived as [7]:

$$H(\mathrm{f}) = [\sum_{-N}^{N} G_k \, \mathrm{e}^{-j\,2\pi fk\,(\tau_g - \tau_d)}]\mathrm{e}^{-j\,2\pi fN\,(\tau_g + \tau_d)} \tag{1}$$

Which $\tau_k = \tau_g - \tau_d$ (τ_k is the delay in Fig.2).

IV. TOPOLOGY OF PROPOSED LINEAR PHASE DISTRIBUTED AMPLIFIER

With regard to the advantage of the CMOS technology which are low cost and integrality, we designed a linear phase distributed amplifier in this technology. As the parasitic capacitors for this technology are larger than those of P-HEMT technology (implemented in [7]), the method introduced in [7] is not applicable in our proposed design method for a wideband linear phase amplifier. To achieve the linear phase response, we used cascaded amplifier in each amplifier stage. Fig. 4 shows the proposed configuration for our linear phase distributed amplifier. In proposed method the gain and delay of each signal path have been optimized to achieve a desired phase response. From these parameters (delays and gains), the gate width of each transistor is obtained.

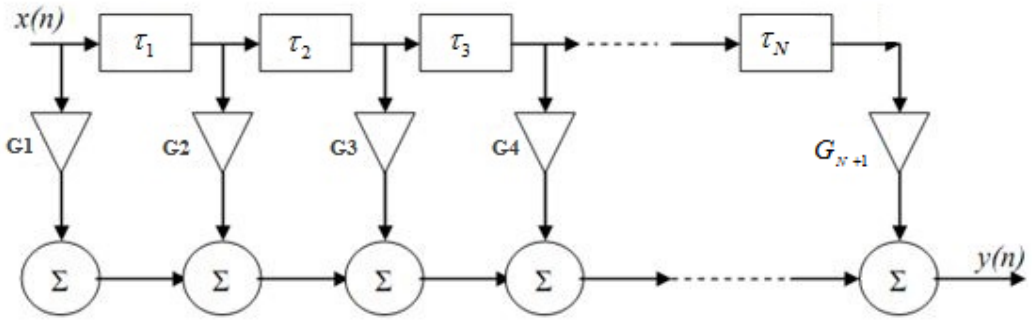


Fig. 2. Topology of generalized transversal filter

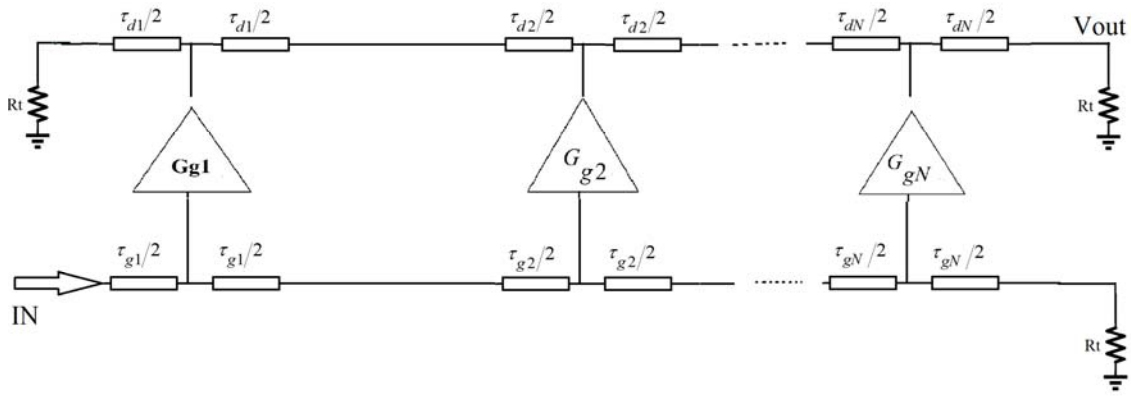


Fig. 3. Distributed amplifier with transversal filter topology

A. Circuit Analysis of the Proposed Method.

Assume the number of stages in the gate and drain lines are N and the number of cascaded transistors in each stage are M. For input signal, the gate voltage of each transistor at gate line can be represented as:

$$Vc_{n1} = V_i [e^{-\sum_{k=1}^{n-1} j2\pi f (\tau_{g_{k1}})}] \quad (2)$$

where, $\tau_{g_{k1}}$ is delay for the first gate line. The induced current in the drain of transistor at *nth* column and *mth* row is as:

$$I_{d_{nm}} = V_{c_{nm}} g_{m_{nm}} \qquad 2 \le m \le M-1 \quad (3)$$

The applied voltage to the gate of transistor at *nth* column and *mth* row can be presented as:

$$V_{c_{nm}} = Z_{d_{n(m-1)}} I_{d_{n(m-1)}} e^{-j2\pi f \tau_{d_{n(m-1)}}} \quad (4)$$

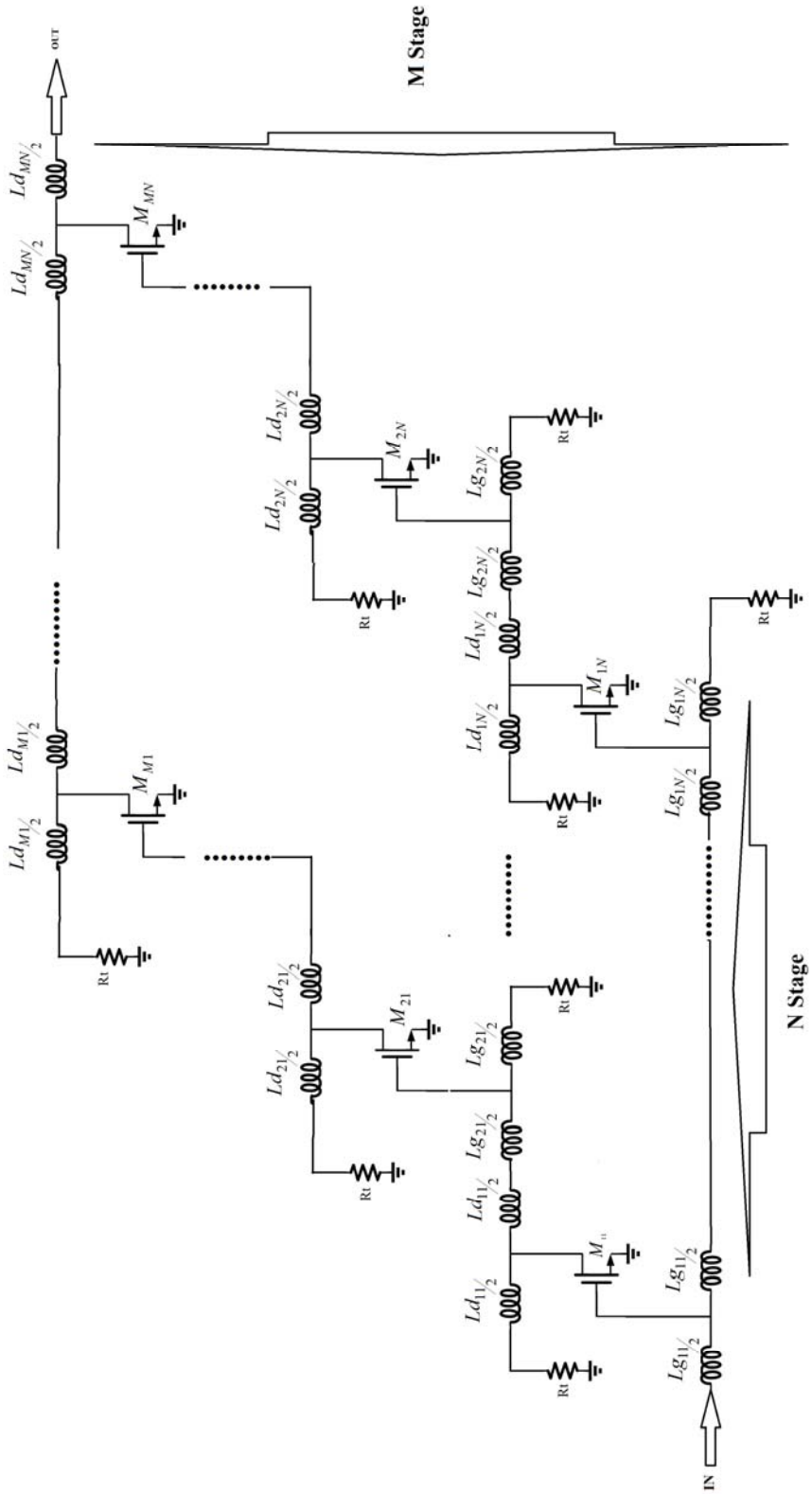


Fig. 4. Topology of the proposed amplifier

Table 1. Gate width of each 5×4 transistor (μm).

parameter	Value	parameter	Value	parameter	Value	parameter	Vlaue
W_{11}	60	W_{21}	115	W_{31}	50.5	W_{41}	51.5
W_{12}	17	W_{22}	70	W_{32}	146	W_{42}	22.5
W_{13}	64	W_{23}	93	W_{33}	92	W_{43}	48.5
W_{14}	57	W_{24}	72	W_{34}	98.5	W_{44}	26
W_{15}	80	W_{25}	80	W_{35}	65.5	W_{45}	43.75

Using the above equations, the induced current in each direction in drain line is in the form of $(-\frac{1}{2}I_{d_{nM}}e^{\pm j\,2\pi f\,\tau_{d_{nM}}})$ where $I_{d_{nm}}=V_{C_{nm}}g_{m_{nm}}$. Therefore, the total output current in Nth terminal of drain line can be shown to be:

$$I_o=-\frac{1}{2}\sum_{n=1}^{N}I_{d_{nM}}e^{-(\mathrm{N}-\mathrm{n})j\,2\pi f\,\tau_{d_{nM}}} \tag{5}$$

Where $\tau_{d_{nM}}$ is drain line delay. If the input/output of the amplifier are matched, the power gain can be calculated as:

$$G=\frac{P_{out}}{P_{in}}=\frac{\frac{1}{2}\left|I_o\right|^2 Z_d}{\frac{1}{2}\left|V_i\right|^2 / Z_g} \tag{6}$$

V. RESULTS

As the relations obtained for gain and group delay in our proposed method are too complicated, we have implemented a MATLAB code and also used ADS software to simulate the gain and phase response of the designed linear phase amplifier. The gain and group delay of the proposed amplifier are shown in Fig. (5-a) and (5-b). As can be seen from these figures, the group delay is flat which means the phase is linear while the gain is also acceptable. The amplifier has 5×4 transistors (5 stage in which each stage consists of 4 cascaded transistors). Table 1 shows the gate width of each 5×4 transistor. Table 2 shows the value of the gate lines inductors and Table 3 shows the value of the drain lines inductors. The graphs S_{11} and S_{22} demonstrating the input and output matching are shown in Fig. 6. As can be seen in Fig. 6, these parameters have been validated by Cadence software. output power for 1 dB compression (P1dB) and Output Third-Order Intercept(OIP3) demonstrating the

Table 2. **V**alue of the gate lines inductors (pH).

parameter	Value	parameter	Value	parameter	Value	parameter	Vlaue
L_{g11}	144	L_{g21}	3	L_{g31}	2	L_{g41}	2
L_{g12}	68	L_{g22}	176	L_{g32}	2	L_{g42}	13
L_{g13}	108	L_{g23}	3	L_{g33}	2	L_{g43}	94
L_{g14}	40	L_{g24}	103	L_{g34}	2	L_{g44}	194
L_{g15}	220	L_{g25}	3	L_{g35}	2	L_{g45}	2

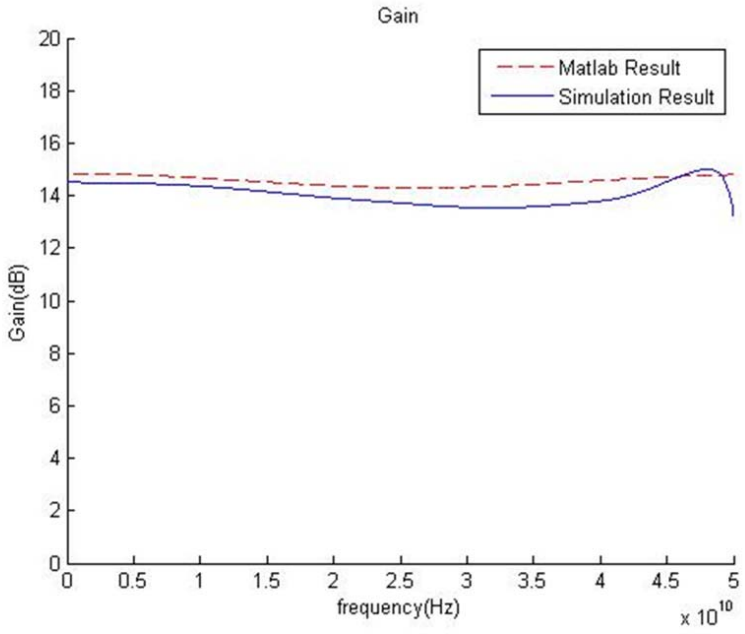
Table 3. Value of the drain lines inductors (pH).

parameter	Value	parameter	Value	parameter	Value	parameter	Vlaue
L_{d11}	296	L_{d21}	298	L_{d31}	480	L_{d41}	410
L_{d12}	3	L_{d22}	380	L_{d32}	500	L_{d42}	68
L_{d13}	349	L_{d23}	292	L_{d33}	7	L_{d43}	434
L_{d14}	8	L_{d24}	436	L_{d34}	402	L_{d44}	106
L_{d15}	184	L_{d25}	346	L_{d35}	374	L_{d45}	300

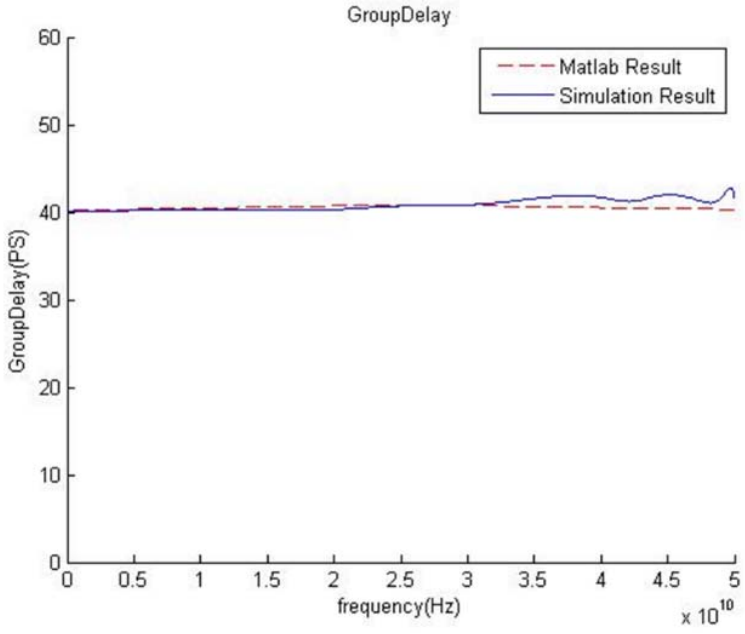
linear circuit performance are shown in Fig. 7. Noise Figure and S12 demonstrating the isolation of the input from the output are shown in Fig. 8. As you can see in Fig. 8 (b), there is a perfect isolation of the input from the output.

VI. CONCLUSION

In this paper a new topology for the design of linear phase distributed amplifier in the frequency range of 0-50 GHz has been proposed. In the proposed method proper weighing factors have been used in different signal paths for 5-stages amplifier which each stage consists of 4 cascaded transistor to obtain the desired linear phase response. Gain and delay of each transistor were obtained using a MATLAB code. The simulated results shows the capability of the proposed method for design and analysis of linear phase distributed amplifier to be used in optical receivers. Finally, a comparison between the work carried out in this paper and the work done in several of the references is presented in Table 4.

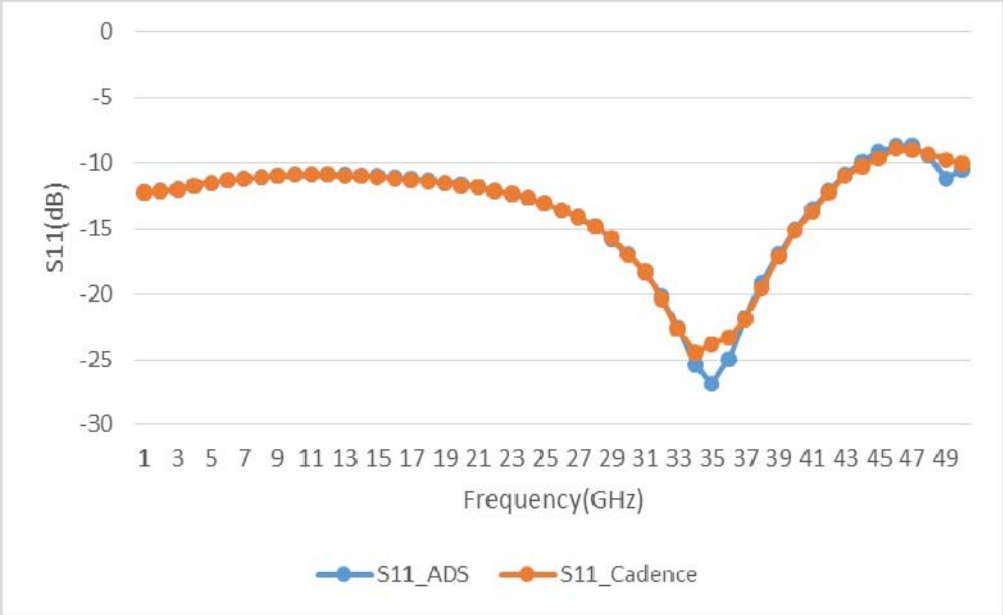


(a)

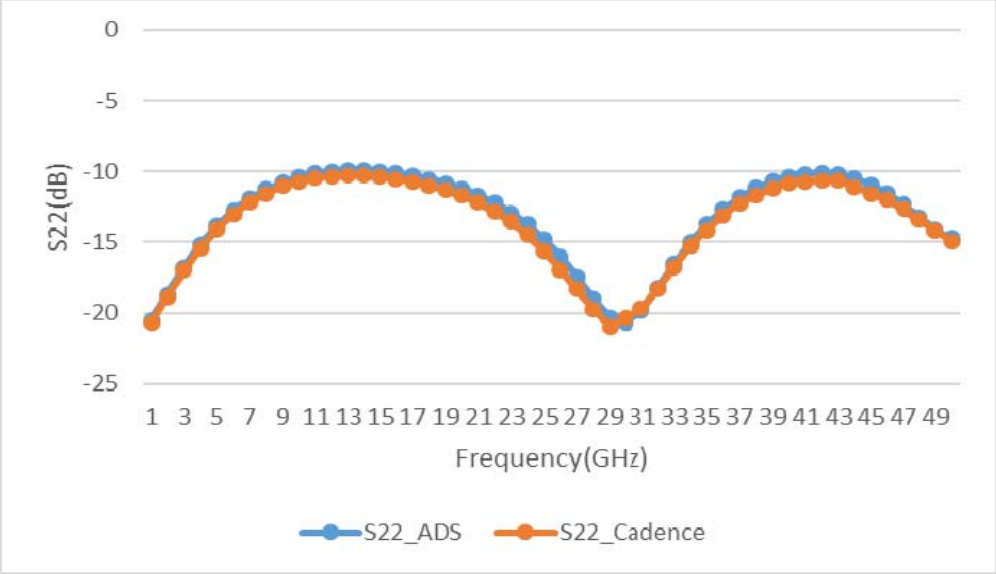


(b)

Fig. 5. Simulated (a) gain and (b) group delay of the proposed amplifier

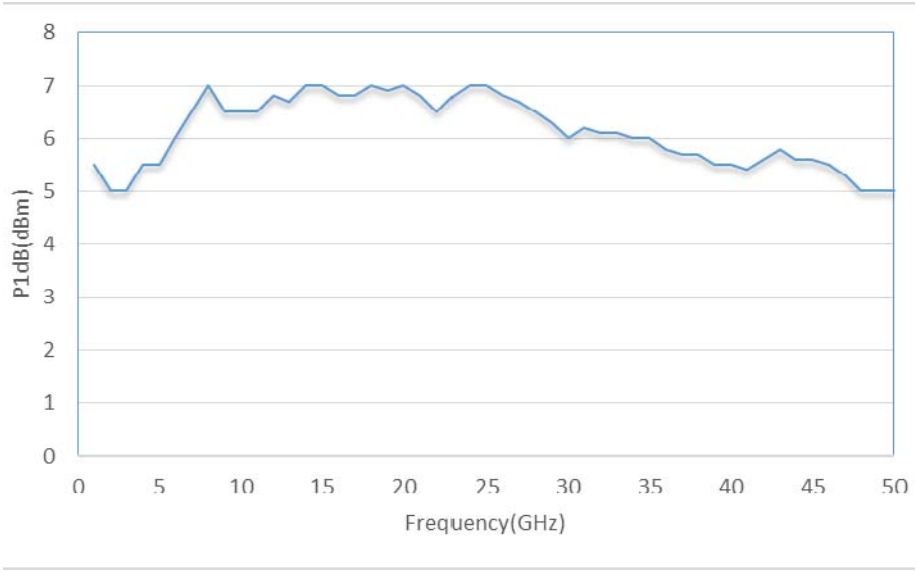


(a)

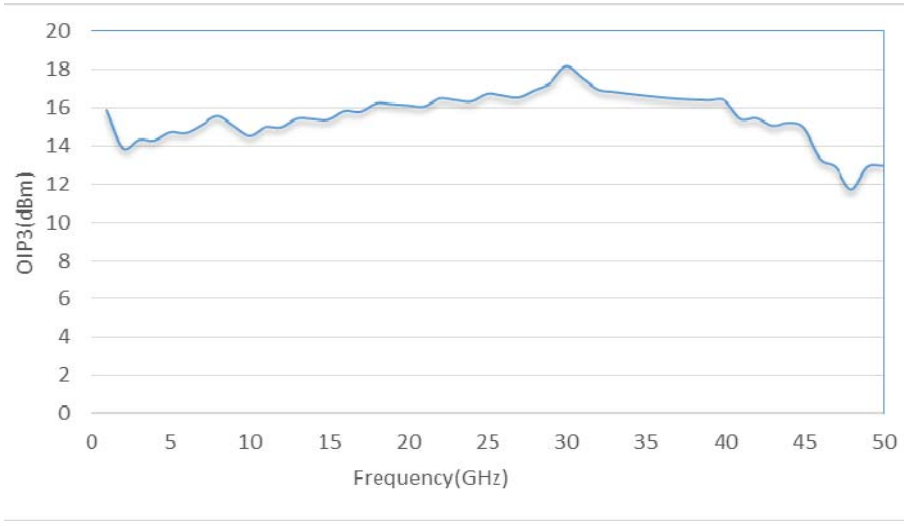


(b)

Fig. 6. Simulated S-Parameters at (a) Input and at (b) output of the proposed amplifier



(a)



(b)

Fig. 7. Simulated P1dB vs. Frequency (a) and Output IP3 vs. Frequency (b) of the proposed amplifier

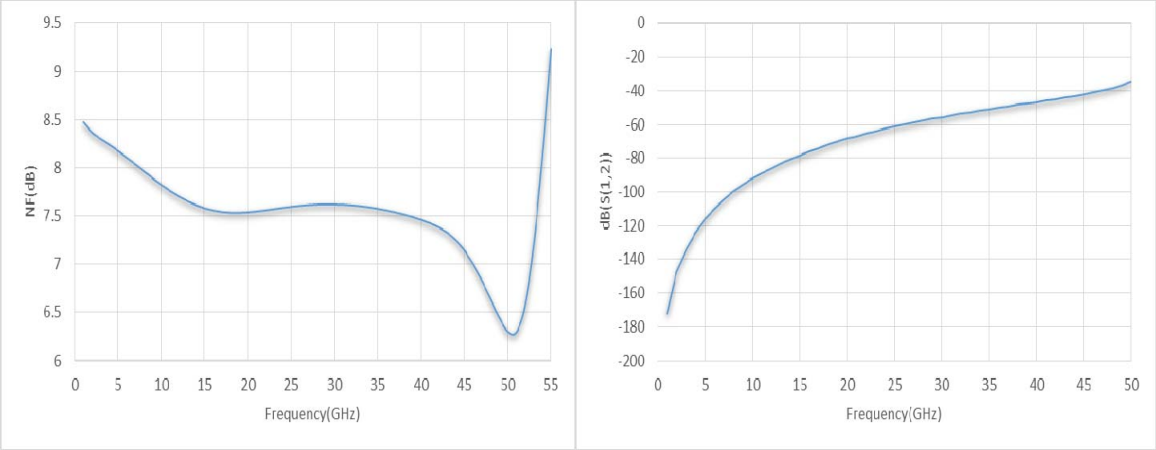


Fig. 8. Simulated (a) Noise Figure vs. Frequency and (b) S12 vs. Frequency of the proposed amplifier

Table 4. Summary of performance and comparison of multiple reference results with the work done in this article

Reference	Technology	Bandwidth(GHz)	Gain(dB)	Input Matching	Output Matching
[8]	CMOS 180	15	---	---	---
[9]	CMOS 180	25	6	---	---
[10]	CMOS 180	30	-5	>-10	>-15
[7]	HEMT	40	10	---	---
This Work	CMOS 180	50	14.5	>-9.5	>-8.7

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