Design and Fabrication of a 9–11 GHz Balanced Low Noise Amplifier Using HJFET

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***Abstract*— This paper describes the design of an X-band balanced low noise amplifier (LNA) using an available HJFET device. The balanced LNA consists of a pair of electrically similar transistors whose input and output signals are divided or combined by 3 dB two-stage Wilkinson power dividers. The proposed balanced LNA is fabricated and measured. The measured results show that the noise figure is 1.30 dB at 10 GHz, the input and output return loss are more than 15 dB and 10 dB, respectively. Also, the gain of 12 dB and gain flatness of ±0.5 dB over the 9-11 GHz frequency range are associated to the balanced LNA. In addition, 15-element small signal equivalent model parameters of the HJFET device used in amplifier design are extracted with an analytical and optimization approache such as Particle Swarm Optimization (PSO) to achieve accurate values. The small-signal model parameters evaluated with the PSO attain 5.9% error compared to the measured data. The validity of the proposed approach is shown by comparing the modeled S-parameter and measured results over 2-18GHz. Simulation results indicate that the PSO approach accurately extracts the small signal model parameters of the HJFET.**

***Index Terms*—** balanced LNA, heterojunction field-effect transistor (HJFET), Wilkinson power divider, Particle Swarm Optimization (PSO), small-signal model.

I. INTRODUCTION

In most of microwave and wireless base station equipment, low noise amplifier (LNA) is used as the first stage of receiver block to ensure proper sensitivity obtained by the whole receiver. The problem in the design of conventional LNA comes from the fact that it has to provide the lowest noise figure possible with high gain and appropriate matching at different frequencies. In addition, the design of a LNA at higher frequency with broad band is performed using special technical approaches. Challal *et al.* [1] designed a two-stage K-band LNA based on microstrip technology. They achieved a noise figure of 1.78 dB, a power gain of 15.37 dB, input and output return loss of 17.34 dB and 22.33 dB, respectively at operating frequency of 24.125 GHz. Also, Waliwander *et al.* [2] designed a LNA using a balanced microstrip structure, it provided noise figure of 3 dB, input and output reflection coefficients better than -13 and -20 dB, respectively and an overall gain around 10dB over the entire UWB band

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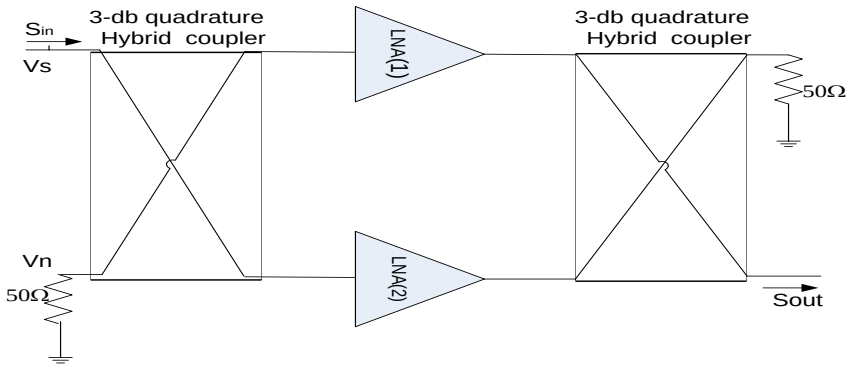


Fig. 1. The configuration of a balanced amplifier [8].

(3.1-10.6 GHz). In another work, Misran *et al.* [3] implemented a LNA for WLAN application using feedback and balanced topology. The proposed LNA resulted in a noise figure less than 2 dB, gain more than 10 dB, and S_{11} and S_{22} less than -10 dB at 2.4 GHz.

The balanced amplifier topology is usually preferred in low noise applications because it comprises several advantages: (1) providing a good input/output impedance matching, (2) improvement of 1dB compression point by 3-dB, (3) higher linearity, (4) good stability and (5) redundancy. Conventionally, a balanced amplifier is realized using two identical amplifiers which are in parallel connected as shown in Fig. 1. The input signal is fed through a 90° hybrid power divider and equally divided and injected into the inputs of the two single-ended amplifiers. The amplified signal at the output of each amplifier then is combined by a 90° hybrid power combiner as the output signal. The reflected signals from two amplifiers at the input or output ports are cancelled because of their out-of-phase property. Balanced amplifiers have been carried out with different types of couplers, such as branch-line coupler [3], Lange coupler [4] and Wilkinson power divider [5]. This paper presents a description of design, fabrication and measurement data of an X-band balanced LNA which is suitable to use in broad band microwave radio repeater stations or radars. 3dB two-stage Wilkinson power dividers are used to implement the balanced LNA with a super low noise amplifier HJFET.

It is used the small signal model of HJFET instead of S2P file to design of the amplifier. An exact small signal circuit parameters of a FET (MESFET or HJFET) are normally extracted using either optimization or analytical techniques. A new analytical method was developed to extract the parasitic elements of GaN devices that used cold S-parameter measurements for the extrinsic parameters [6]. Mengistu used un-biased FET instead of gate-forward biasing condition to extract the parasitic inductances and resistances [7]. Since the optimization of all small signal parameters is heavy and rigorous by custom optimization techniques, so it is necessary to find initial values of parameters with an analytical approach. Here, small signal parameters are first extracted using analytical technique then the initial values optimized with PSO technique. The remainder of the paper is organized as follows. In section II, the design of the 3dB two-stage Wilkinson power divider is presented. A brief description

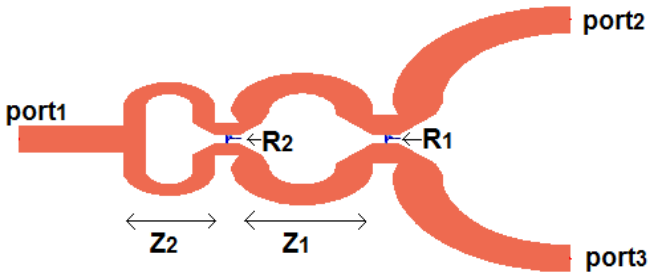


Fig. 2. Layout of the implemented 2-stage wilkinson power divider.

TABLE I. THE PARAMETER VALUES OF THE 3DB 2-STAGE WILKINSON POWER DIVIDER.

Parameters	**Value**	**Parameters**	**Value**
R1 (Ω) R2(Ω)	200 100	Z1 (Ω) Z2(Ω)	60 83.35

of the small-signal model parameter extraction is explained in section III. Design of the balanced LNA is provided in section IV, and then the simulated predictions and measured results are stated in section V. Finally, the paper is concluded in the last section.

II. IMPLEMENTATION OF A 2-STAGE WILKINSON POWER DIVIDER

The design of a balanced amplifier requires an extra step to design the coupler besides the DC-biasing network. We adopted a balanced amplifier configuration by two 2-stage Wilkinson power dividers. The power divider is implemented as the circuit configuration shown in Fig. 2. The VSWR characteristics of the balanced amplifier is much dependent on the power divider. The 3dB two-stage Wilkinson power divider is designed at center frequency of 10 GHz. RT-Duroid-5880 with ε_r=2.2 and 20 mil thickness is used as the substrate. The essential dimensions of the two-stage power divider are the values of bridging resistors R_1 and R_2 and transmission lines with characteristics impedance Z_1 and Z_2, which their values are given in Table I [9]. Electrical length of transmission lines are obtained with Smith Chart Utility tool of ADS software. Then, linecalce tool of ADS software is used to obtain their physical lengths. Finally, these values are tuned for the power divider configuration using optimization tools of ADS software. The simulated results from momentum tool of ADS software are depicted in Fig. 3. The results indicate that the reflection efficient of port 1 is less than -22.7 dB also the insertion loss is 3.075 dB throughout the entire frequency range of 9-11 GHz.

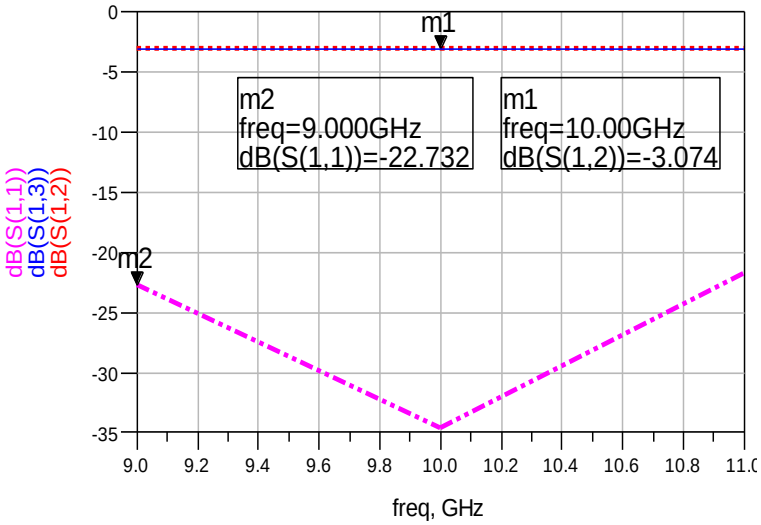


Fig. 3. Momentum simulation results of the implemented 3dB two-stage wilkinson power divider.

III. SMALL- SIGNAL MODELING OF THE TRANSISTOR

The accurate small-signal modeling of a HJFET device used in design of an amplifier is normally carried out using both optimization and analytical techniques. The 15-element small-signal equivalent circuit shown in Fig. 4 is widely used to indicate electrical linearity behavior of HJFET divices over entire range of frequencies at a specific bias point [7]. The circuit consists of two parts; the extrinsic part includes bias-independent elements such as $C_{pd,}$ C_{pg}, $R_{d,}$ $R_{g,}$ R_s, L_g, L_s, and L_d and bias-dependent intrinsic part consists of the parameters g_m, C_{gs}, C_{gd}, R_i, R_{ds}, C_{ds} and τ. These parameters are extracted from the measured S-parameters as follows. First, the extrinsic parameters are extracted based on the measured S-parameters data under cold pinch-off bias conditions, *i.e.* $V_{GS}<V_p$ and $V_{DS}=0V$ [6]. In the second stage, the extrinsic resistances are extracted from the measured S-parameters data under un-bias condition ($V_{GS}=0V$, $V_{DS}=0V$) [10]. Finally, the intrinsic parameters are extracted from the measured S-parameters under hot-bias condition ($V_{DS}>0V$, $V_{GS}<0V$) [6], and [7]. The intrinsic parameters are evaluated from the de-embedded extrinsic parameters of equivalent circuit Y-parameters. The inner parameters are derived from equations (1) to (12) using S-parameters of the transistor at $V_{DS}=2V$ and $V_{GS}=-0.25V$ bias point (from 2 to 18 GHz) [11].

$$Y_{i,11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \quad (1)$$

$$Y_{i,12} = -j\omega C_{gd} \quad (2)$$

$$Y_{i,21} = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} - j\omega C_{gd} \quad (3)$$

$$Y_{i,22} = g_d + j\omega(C_{gd} + C_{ds}) \quad (4)$$

$$D = 1 + \omega^2 C_{gs}^2 R_i^2 \quad (5)$$

Note that Y_i denotes Y-parameter of the intrinsic part of the equivalent circuit. Therefore, the small-signal model parameters are

$$C_{gs} = \frac{\left|Y_{i,11} + Y_{i,12}\right|^2}{\omega \,\mathrm{Im}(Y_{i,11} + Y_{i,12})} \quad (6)$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{i,12})}{\omega} \quad (7)$$

$$R_i = \frac{\mathrm{Re}(Y_{i,11})}{\omega C_{gs}\,\mathrm{Im}(Y_{i,11} + Y_{i,12})} \quad (8)$$

$$g_m = \left|Y_{i,21} - Y_{i,12}\right| \quad (9)$$

$$\tau = -\frac{1}{\omega}\tan^{-1}\left(\frac{\mathrm{Im}(Y_{i,12} - Y_{i,21})}{\mathrm{Re}(Y_{i,12} - Y_{i,21})}\right) \quad (10)$$

$$G_{ds} = \mathrm{Re}(Y_{i,22}) \quad (11)$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{i,22})}{\omega} - C_{gd} \quad (12)$$

Finally, the 15-element small-signal equivalent model parameters of AlGaN/GaN HJFET device are evaluated with an analytical procedure. Then, these values are used as initial values for an optimization technique such as particle swarm optimization (PSO) to achieve accurate values over entire range of frequency between 2 to 18 GHz [12], and [13]. The objective function is sum of square errors between the simulated and measured S-parameter values [6].

$$\varepsilon_{ij} = \frac{\left|\mathrm{Re}(\delta S_{ij,n})\right| + \left|\mathrm{Im}(\delta S_{ij,n})\right|}{w_{ij}} \quad \text{i, j = 1, 2, and n = 1,2,....,N} \quad (13)$$

$$w_{ij} = \max\left|S_{ij}\right|,\ i, j = 1,2 \quad i \neq j \quad (14)$$

$$w_{ii} = 1 + \left|S_{ii}\right|,\ i = 1,2 \quad (15)$$

$\delta S_{ij,n}$ is the difference between measured and simulated S-parameters at each operating frequency f_n. N is the number of measured data points and w_{ij} is a weighting factor. So, the scalar S-parameter fitting error ε_s is defined as

$$\varepsilon_s = \frac{1}{N}\sum_{n=1}^{N}\left\|\varepsilon(f_n)\right\|_1 \quad (16)$$

$$\varepsilon(f_n) = \begin{bmatrix} \varepsilon_{11}(f_n) & \varepsilon_{12}(f_n) \\ \varepsilon_{21}(f_n) & \varepsilon_{22}(f_n) \end{bmatrix} \quad (17)$$

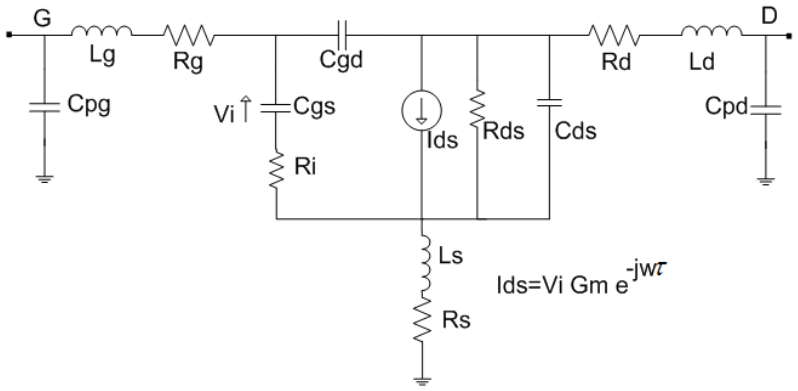


Fig. 4. The small-signal equivalent circuit of a HJFET.

Since HJFET devices are often used to the design of power amplifier the stability factor and amplifier gain are important to be considered. These factors can be expressed in form of a function of S-parameters which can be used during the PSO procedure. The fitting error of the stability factor is

$$\varepsilon_{\mathrm{k}} = \frac{1}{N}\sum_{k=1}^{N}\left|K_{meas} - K_{sim}\right| \tag{18}$$

K_{meas} and K_{sim} are the stability factor from the measured and simulated S-parameters, respectively [11]. In addition, the fitting error of the gain can be expressed as

$$\varepsilon_{\mathrm{G}} = \frac{1}{N}\sum_{m=1}^{N}\left|G_{meas} - G_{sim}\right| \tag{19}$$

G_{meas} and G_{sim} are the gain from the measured and simulated S-parameters, respectively [11]. So

$$\varepsilon_{\mathrm{G}} = \frac{1}{N}\sum_{m=1}^{N}\left|\frac{\left|S_{21}^{meas}\right|^2 - 1}{\ln\left|S_{21}^{meas}\right|^2} - \frac{\left|S_{21}^{sim}\right|^2 - 1}{\ln\left|S_{21}^{sim}\right|^2}\right| \tag{20}$$

Ultimately, the objective function is given as

$$\varepsilon = \sqrt{\frac{1}{3}(\varepsilon_s^2 + \varepsilon_k^2 + \varepsilon_G^2)} \tag{21}$$

The three components of (21) are calculated from the S-parameters, the objective function is then minimized using the PSO method.

The results for the HJFET given in Table II show the S-parameter values obtained with PSO has 5.9% error compared to the measured data. Fig. 5 indicates the comparison of the measured and modeled S-parameters vs. frequency for the real and imaginary parts of S_{11}, S_{12}, S_{21} and S_{22}, at V_{DS} = 2V and V_{GS} = -0.25V bias point. This bias point is used to design of the balanced amplifier. The

Table II. Comparison of the extracted elements of the chosen HJFET.

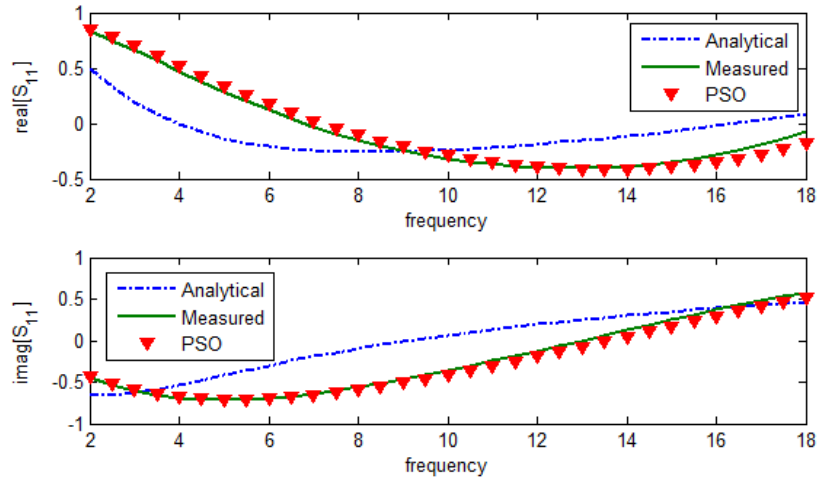
Parameters	**Initial Value**	**Search range(min)**	**Search range(max)**	**PSO**
				2.055
Rs (Ω)	1.048	1	3.5	4.69
R_d (Ω)	2.59	2	5.5	3.51
R_g (Ω)	1.233	0.9	5.5	116.34
L_s (pH)	144	70	350	562.56
L_g (pH)	478	450	700	572.2
L_d (pH)	543	350	700	73.46
C_{pd} (fF)	110	50	150	63.72
C_{pg} (fF)	52.218	20	100	25.62
C_{gd} (fF)	23.74	1	80	0.226
C_{gs} (pF)	0.663	0	1	122.58
C_{ds} (fF)	125.79	100	200	1.06
R_i (Ω)	14.83	0.1	20	90
G_m (mmho)	141.55	100	190	3.166
τ (ps)	0.3649	0	6	216.415
R_{ds} (Ω)	128	120	400	
Error	**1.21**			**0.059**

proposed PSO technique assures good accuracy and reliability in the parameter extraction of the HJFET device. Excellent agreement is obtained between modeled and measured S-parameters for the AlGaN/GaN HJFET device over a wide range from 2GHz to 10 GHz. The results indicate the consistency and accuracy of the approach.

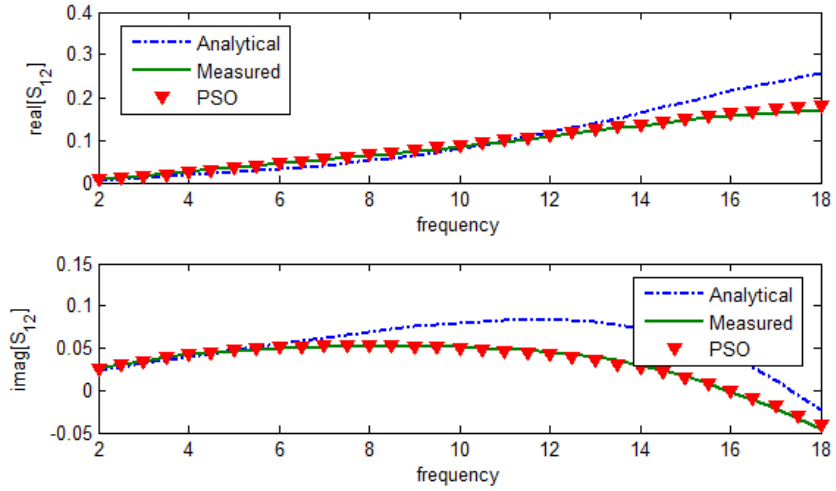
IV. DESIGN OF THE BALANCED LNA

As seen in Fig. 1, the balanced LNA design is dependent on the use of single-ended low noise amplifiers. The super low noise and high gain AlGaN/GaN HJFET stated in the previous section is employed to realize the amplifier. The HJFET is biased at V_{DS}=2V and I_{DS}=20mA to realize high gain and low noise figure. The scattering parameters of the HJFET at this bias point at 10 GHz have been depicted in Fig. 5.

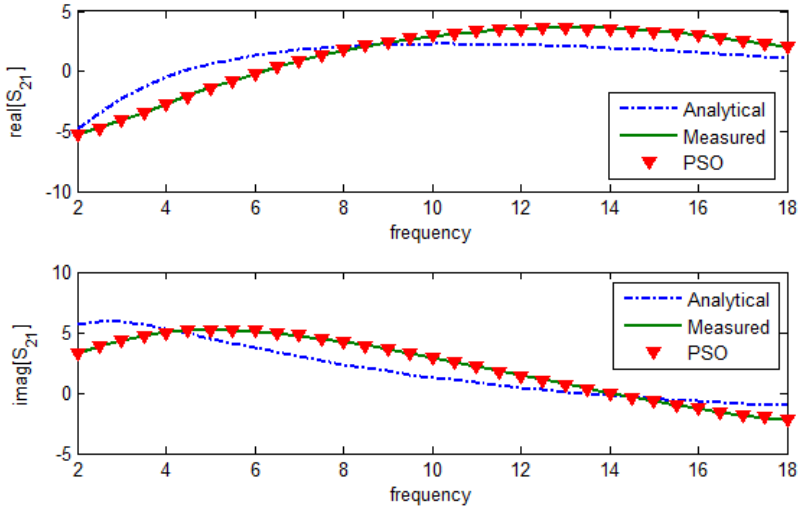
The input and output matching networks are designed to achieve minimum noise figure and flat and high gain over frequency range of 9-11 GHz. So, each single-ended LNA is preferred to design for the lowest noise and highest gain rather than for the minimum input/output standing wave ratios. The simulated results for single-ended LNAs are shown in Figs. 6 and 7. The noise figure and the gain of the single-ended amplifier are about 0.56 dB and higher than 12.2 dB in the entire frequency range of interest, respectively. Although the input and output reflection coefficients are high due to the fact that



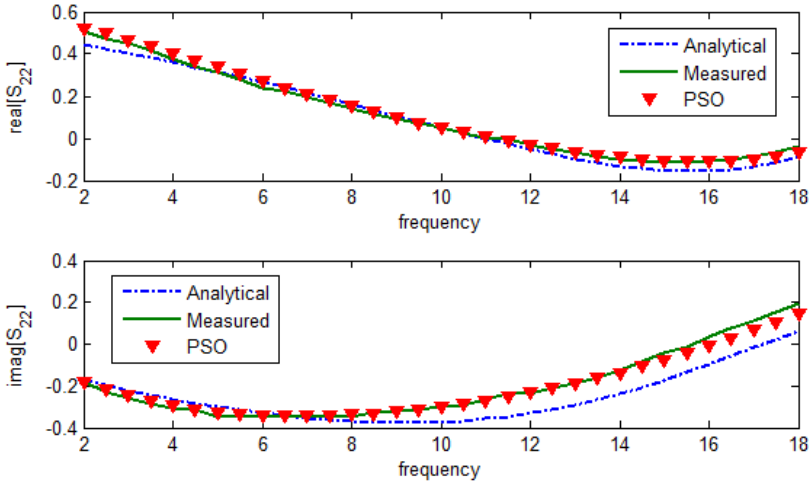
(a) Real and imaginary part of S_{11}



(b) Real and imaginary part of S_{12}

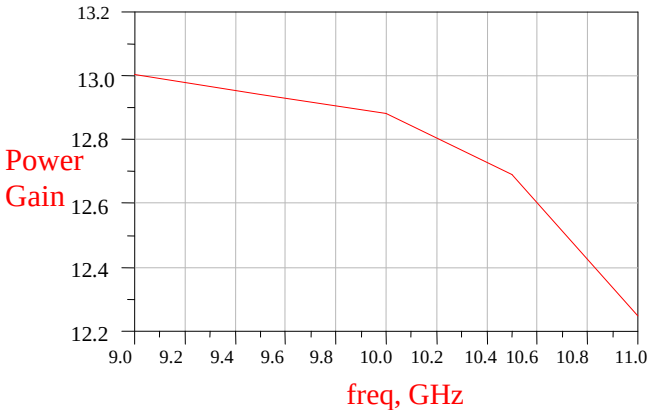


(c) Real and imaginary part of S_{21}



(d) Real and imaginary part of S_{22}

Fig. 5. Comparison of the measured and modeled real and imaginary part of S-parameters vs. frequency at VDS = 2V and VGS = - 0.25V bias point and 10 GHz using the analytical and PSO techniques.



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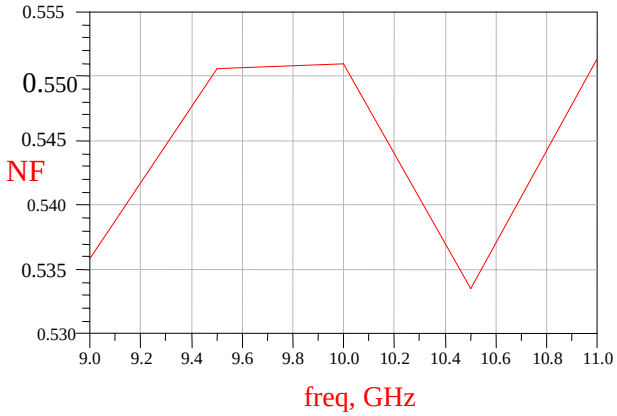
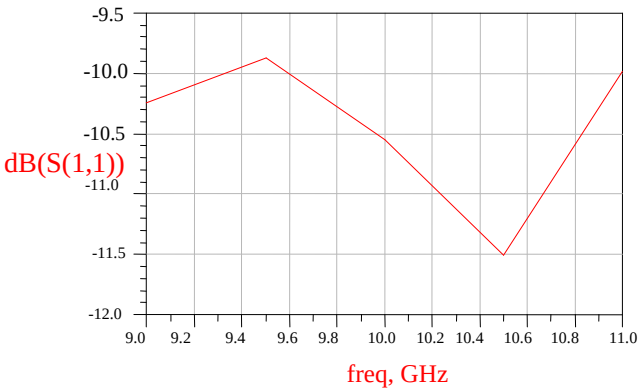


(b)

Fig. 6. Simulation results of the gain and noise figure of the single-ended LNA.

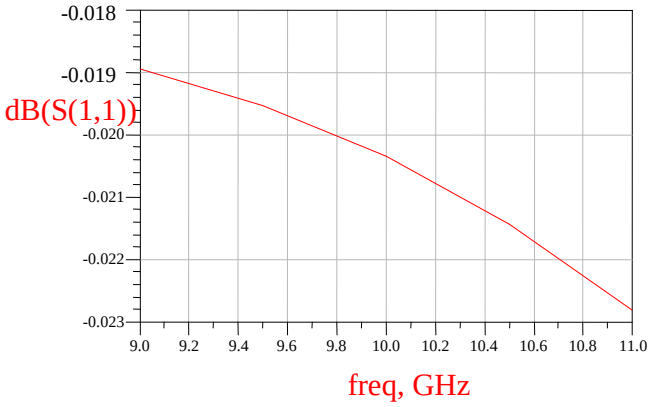


(a)

(b)

Fig. 7. Simulation results of the input/ouput reflection coefficients of the single-ended LNA.

major attention was placed on the low noise and high gain of the LNA. Then, two identical single-ended amplifiers and additional quarter wave transformers with two 3dB two-stage Wilkinson power dividers are used to design the balanced LNA [8]. The balanced LNA is implemented on the RT-Duroid-5880 with ε_r=2.2 and 20 mil thickness. Two-stage Wilkinson power/combiner dividers are, designed in section II, used to match source and load impedance to 50Ω. However, the dimensions of the matching networks are optimized in the final layout of the single-ended LNA. The additional quarter wave transformers at the input of LNA (A_1) and output of LNA (A_2) are used to provide 90° phase difference at output ports of power dividers. Furthermore, additional notch filters are added in the balanced amplifier configuration to improve the isolation between RF and DC path. The bias connection acts as leakage path for the high frequency signal. So, isolation is required at the operating frequency in order to prevent the signal from leaking out into the bias port. An important point to be considered is the bandwidth of filter, which should include the RF input bandwidth [13]. To design of the notch filters, two butterfly radial stubs are used together with the quarter wavelength microstrip line. The radial stubs are used in order to achieve a high attenuation with good stop band as wide as possible [14]. The performance of the filter at the frequency range is shown in Fig. 8. As shown, the attenuation over the stop band is larger than 54dB over frequency range of 9-11 GHz.



(a)

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Fig. 8. Reflection and transmission coefficient of the proposed notch filter, port 1 is RF-port and port 2 is DC-port.

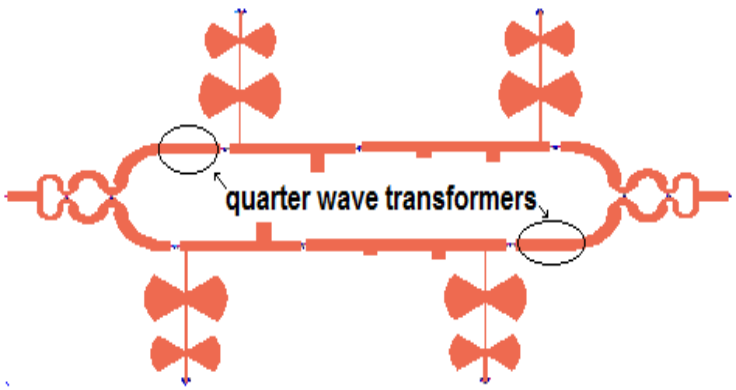


Fig. 9. Layout of the proposed balanced LNA.

Finally, the balanced LNA circuit is optimized by ADS software to obtain the design goals. Very little tuning is necessary to achieve the desired response. The physical layout of the balanced LNA is shown in Fig. 9.

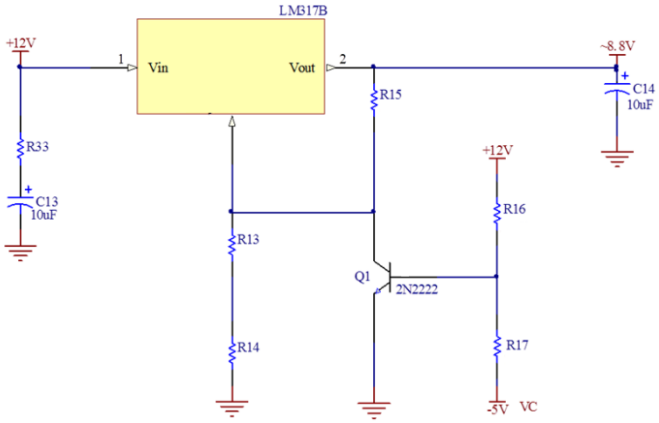
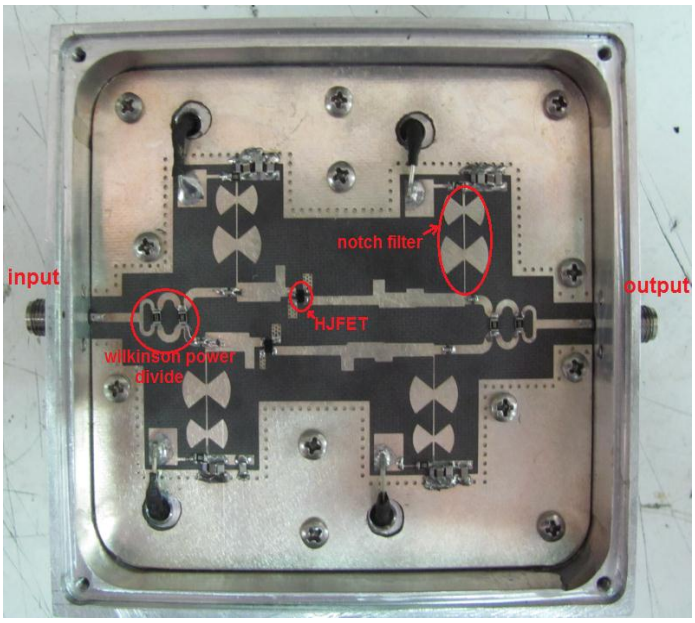


Fig. 10. Topology of the active bias network.

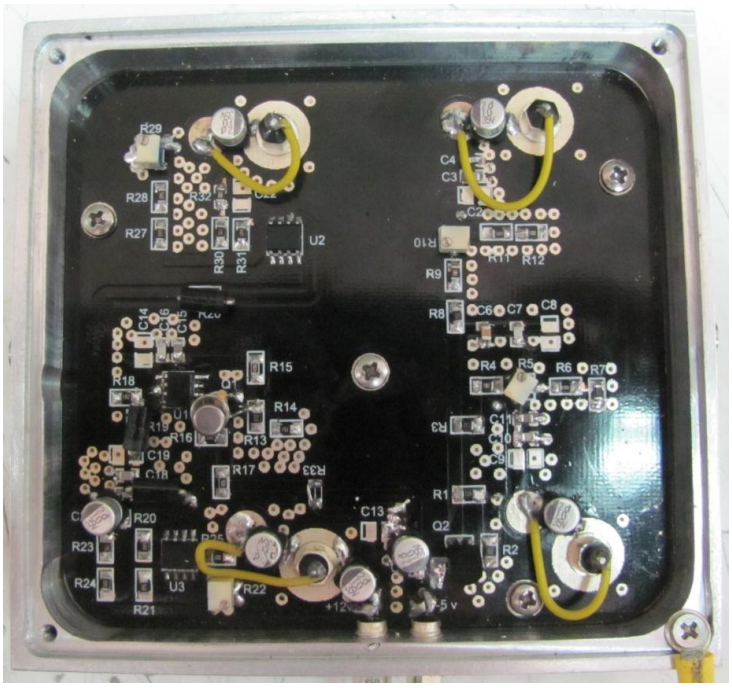
I. FABRICATION AND MEASUREMENTS OF THE BALANCED LNA

The balanced LNA is fabricated on the substrate of RT-Duroid-5880 with a dielectric constant of 2.2, and thickness of 20 mil. The circuit layout is designed to fabricate with Altium designer release 10. The circuit is fed by a dual supply of -5V and +12V through the two DC pins. Note that the DC-biasing circuit is designed to protect the balanced LNA from reverse biasing. In addition, an active bias network is used to protect the LNA when the Drain is biased earlier than gate as shown in Fig. 10. The biasing circuit is supplied by -5V and 12V. LM317B regulator in the circuit is used to generate +8.8V to drive two LM317B regulators to excite the drains of the transistors. If VC is connected to -5V firstly before using +12V we have 8.8V to generate drain voltages and the transistors turn on normally without any damage. However, If VC is connected to -5V after using +12V or VC is grounded or floated accidently the output voltage of the circuit is much lower than 8.8 V which results in not turning on the transistors. It should be noted that -5V is used to generate required voltage for the transistors gates in another circuit by LM337B regulator. The DC-biasing network circuit is implemented on a separate FR4 board and mounted on the back of the balanced LNA inside an aluminum box. A metallic sheet is put between them to provide an EMI shielding. With the -5V supply, the current measured at the drain of the circuit is 20 mA which is equal to the simulated circuit. Finally, two 3.5 mm SMA connectors are connected at the input and output ports of the circuit. The photograph of the fabricated balanced LNA is shown in Fig. 11.

The measurements of the balanced LNA are performed by network analyzer. Fig. 12 shows the simulated and measured results of S-parameters from 8.5 to 11.5 GHz. The input return loss is higher than 15 dB and the output return loss is higher than 10 dB in the whole range of 9-11 GHz. It illustrates that the fabricated amplifier is properly matched at the input and output ports. Fig. 12a indicates that



(a)



(b)

Fig. 11. The fabricated balanced LNA (a) RF circuit (b) DC-biasing circuit .

the measured results of S_{11} followed the simulated results. Also, it is observed that the balanced configuration improves the input and output return loss comparing with Fig. 7. The measured gain of the balanced LNA is 12 dB as shown in Fig. 12c and it is 1 dB lower than the simulated results over the whole frequency range of 9-11 GHz. In addition, the gain flatness of the balanced LNA is about ±0.5 dB. The measured results of S_{12} show that the input of the amplifier is well isolated from the output. In

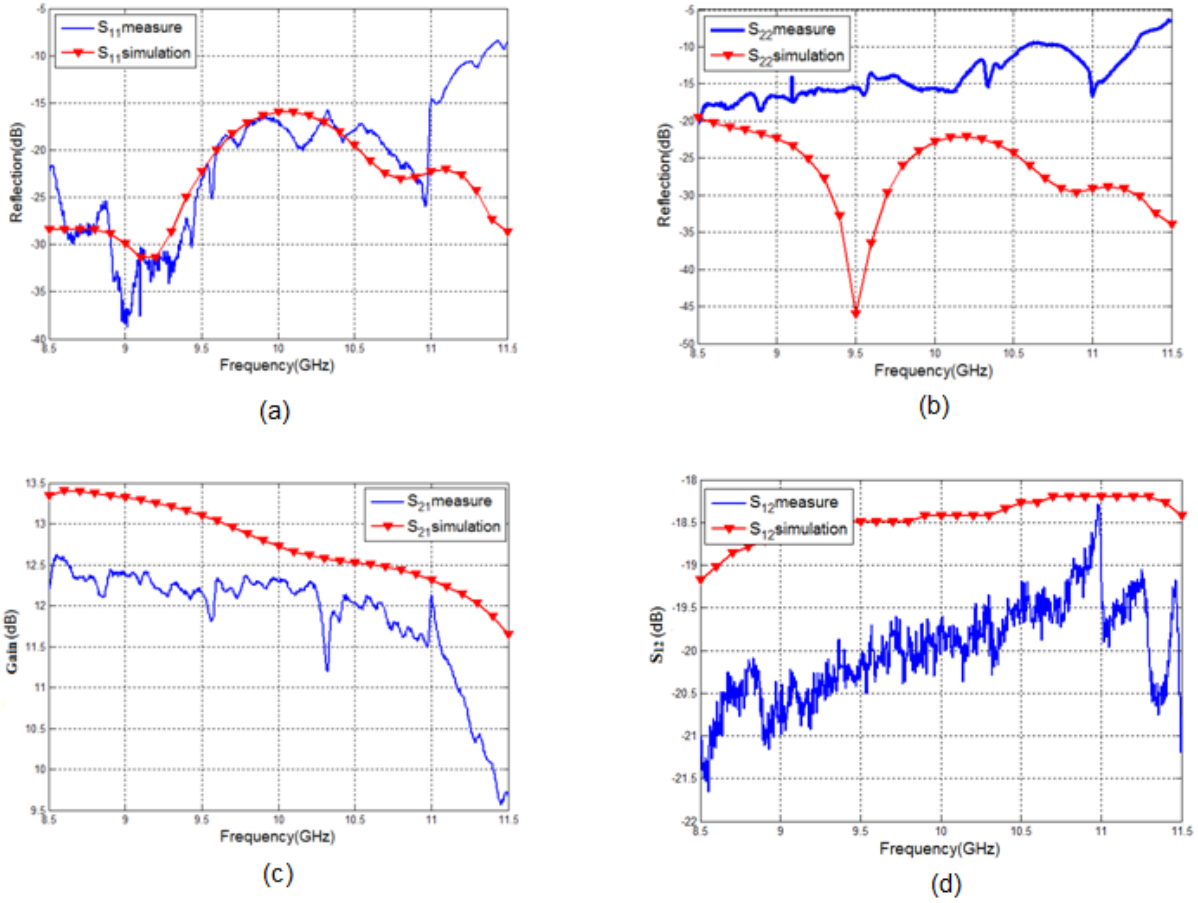


Fig. 12. Comparison of simulated and measured S-parameters of the fabricated amplifier.

all the graphs of Fig. 12, there are some differences between the measured and simulated results which may be pertinent to the effect of input and output connectors and the implementation method.

There are different methods for noise figure measurement such as twice power method, direct noise measurement method, cold source and Y-factor method [15, 16]. The Y-factor method relying on a series of power measurements is suited to low-level noise measurement. The block diagram of the Y-factor method is shown in Fig. 13. A noise source that can be switched off and on is used for the Y-factor measurement. Two power measurements are performed with the same port impedances and the same bandwidth using a RF receiver.

The Y-factor is defined as the ratio of N_{on} to N_{off} which are the output noise power when the noise source are switched on and off, respectively.

$$Y = \frac{N_{on}}{N_{off}} = \frac{kTB\,ENR\,G + N_A}{kTB\,G + N_A} \qquad (22)$$

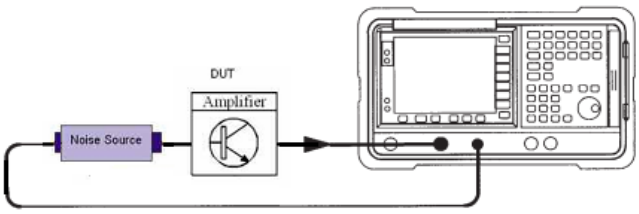


Fig. 13. Block diagram of the noise figure measurment set-up.

Where T refers to the ambient temperature in degrees Kelvin, B to the system bandwidth in Hertz, and k to Boltzman's constant. The excess noise ratio (ENR) is the ratio of noise from the source to the system thermal noise or kTB, often expressed in dB. Also, G is the gain of device under test (DUT) and N_A is the noise power added by the DUT. The noise figure of the DUT is computed by taking the ratio as follows.

$$NF = 1 + \frac{N_A}{kTBG} \tag{23}$$

Using equations (22) and (23), and a few mathematical manipulations, we obtain the desired noise figure (NF) [16].

$$NF = \frac{ENR - 1}{Y - 1} \tag{24}$$

Therefore, making a noise figure measurement using the Y-factor method involves three steps. The first step, often called the calibration step, is to characterize the noise behavior of the RF receiver without the DUT. Two power measurements are obtained by the receiver with the noise source turned OFF and ON. The second step is to make a noise figure measurement on the cascaded the receiver and the DUT. Again, two power measurements are made at the DUT output with the noise source turned OFF and ON. The last step is to de-embed the two measurements. Finally, the NF of the DUT is obtained.

Using the Y-factor method, the noise figure of the balanced LNA is obtained 1.30 dB at 10 GHz. The measured NF at 11 frequency points over frequency range of 9 to 11 GHz is depicted in Fig. 14. In addition, the simulated noise figure of the balanced LNA is shown in Fig. 15. There is a significant increase in the noise figure of the balanced LNA regarding to the simulated results due to the board implementation, the proposed circuit topology and other parasitic components. The results show that the balanced LNA not only improves the return loss, but also leads to a flat gain response regarding to the single-ended LNA. There is not observed any oscillation in the output port even in the case of open-circuit loading.

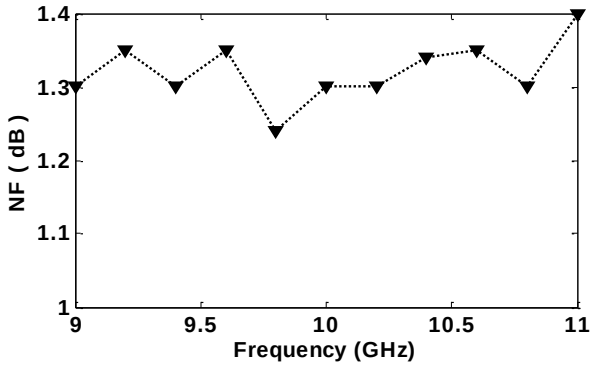


Fig. 14. Measured noise figure of the balanced LNA by Y-factor method.

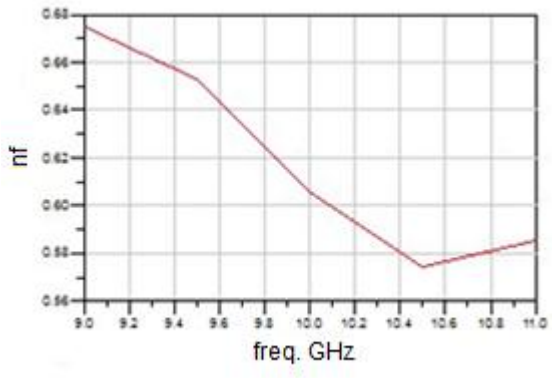


Fig. 15. Simulated noise figure of the balanced LNA.

II. CONCLUSION

A kind of balanced LNA using 3dB two-stage Wilkinson power dividers and a super wide band HJFET was simulated with ADS software and was fabricated on RT-Duroid-5880 substrate. The measured results which have been compared with the simulated show good agreement. The measured results show an excellent noise figure of 1.30 dB at 10 GHz. The input return loss is higher than 15 dB and the output return loss is higher than 10 dB over the whole range of 9-11GHz. The gain is higher than 12 dB with a flatness gain of ±0.5 dB over the entire frequency range of 9-11 GHz. The design is observed to be unconditionally stable over the full frequency band.

In addition, the extraction of a 15-element small-signal model was proposed for HJFET devices and the parameters were obtained for the selected HJFET to use for the amplifier design. The model parameters calculated with a hybrid of analytical and optimization techniques. The simulation results demonstrate that this approach can preciesely extract the 15-element small signal model parameters of the HJFET device. The efficiency of this approach is illustrated by excelent agreement between the

modeled and measured S-parameters data for the HJFET device over a wide frequency range from 2GHz to 10 GHz.

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